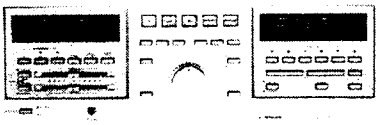
PIONEER®

Service Manual



ORDER NO.
ART-543-0

Quartz SYNTHESIZED STEREO RECEIVER

SX-D7000

MODEL SX-D7000 COMES IN TWO VERSIONS DISTINGUISHED AS FOLLOWS:

Type	Voltage	Remarks
KU	120V only	U.S.A. model
S/G	110V, 120V, 220V and 240V (Switchable)	U.S. Military model

This service manual is applicable to the KU type. When repairing the S/G type, please see the additional service manual (see pages 59 – 69).

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ADDITIONAL SERVICE MANUAL FOR S/G TYPE 59

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Printed in Japan

1. SPECIFICATIONS

Power Amplifier Section

Continuous power output of 120watts* per channel, min., at 8ohms from 20Hertz to 20,000 Hertz with no more than 0.005% total harmonic distortion.

Total Harmonic Distortion (20 Hertz to 20,000 Hertz, 8 ohms)
- continuous rated power output ..... No more than 0.005%
- 60 watts per channel power output ..... No more than 0.004%

Intermodulation Distortion (50 Hertz : 7,000 Hertz = 4:1)
- continuous rated power output ..... No more than 0.005%
- 60 watts per channel power output ..... No more than 0.004%

Frequency Response .... 3 Hertz to 450,000 Hertz $^{+0}_{-3}$dB

Input Sensitivity/Impedance (POWER AMP IN) ..... 1V/50 kilohms

Output
- Speaker ..... A,B,C, A+B, B+C, A+C

Damping Factor (20 Hertz to 20,000 Hertz, 8 ohms) 60

Hum and Noise (IHF, short-circuited, A network) 115dB

Preamplifier Section

Input (Sensitivity/Impedance)
- PHONO 1, 2 MM ..... 2.5mV/50 kilohms
- PHONO 1, 2 MC ..... 0.25mV/100 ohms
- AUX, TAPE PLAY 1, 2, ADAPTOR IN ..... 150mV/50 kilohms

Phono Overload Level (T.H.D. 0.005%, 1,000 Hertz)
- PHONO 1, 2 MM 200mV

Output (Level/Impedance)
- TAPE REC 1, 2, ADAPTOR OUT 150mV
- PREAMP OUT (R_L : 50 kilohms) ..... 1V/1 kilohms (Volume : max)

Total Harmonic Distortion (20 Hertz to 20,000 Hertz)
- PHONO MM 1, 2 → REC OUT ..... No more than 0.005% (4V output)
- AUX, TAPE PLAY 1, 2, ADAPTOR IN ..... No more than 0.005% (4V output)

Frequency Response
- PHONO 1, 2 MM (RIAA Equalization) ..... 20Hz to 20,000 Hertz±0.2dB
- AUX, TAPE PLAY 1, 2, ADAPTOR IN ..... 5Hz to 100,000 Hertz $^{+0}_{-3}$dB

Tone Control
- BASS ..... ±8dB/±10dB (100Hz)
  - Turnover Frequency: 200Hz/400Hz
- TREBLE ..... ±10dB/±8dB (10kHz)
  - Turnover Frequency: 2.5kHz/5kHz

Low Filter 18Hz (6dB/oct.)

Loudness Contour (Volume control set at –40dB position) ..... +6dB (100Hz), +3dB (10,000Hz)

Hum and Noise (IHF, short-circuited, A network)
- PHONO MM/MC 86dB/72dB
- AUX, TAPE PLAY 1, 2, ADAPTOR IN 100dB

Attenuator ..... –20dB

FM Tuner Section

Usable Sensitivity (IHF) 10.2dBf (1.8μV)

50dB Quieting Sensitivity
- MONO 15.7dBf (3.2μV)
- STEREO 34.2dBf (28.2μV)

Signal-to Noise Ratio (at 85 dBf)
- MONO 82dB
- STEREO 78dB

Distortion (at 65dBf)
- MONO 100Hz 0.1%
- MONO *1kHz 0.07%
- MONO 6 kHz 0.1%
- STEREO 100Hz 0.2%
- STEREO 1kHz 0.1%
- STEREO 6kHz 0.2%

Capture Ratio 1.0dB

Alternate Channel Selectivity
- 400kHz 80dB

Stereo Separation
- 1kHz 50dB
- 30Hz to 15kHz 35dB

Frequency Response ..... 30Hz to 15kHz±0.5dB

Spurious Response Ratio 80dB

Image Response Ratio 80dB

IF Response Ratio 90dB

AM Suppression Ratio 60dB

Subcarrier Product Ratio 65dB

SCA Rejection Ratio 65dB

Muting Threshold 35.7dBf (32μV)

Antenna Input ..... 300 ohms balanced, 75 ohms unbalanced

AM Tuner Section

Sensitivity (IHF, Ferrite antenna) 300μV/m
(IHF, Ext. antenna) 15μV
Selectivity 30dB
Signal-to-Noise Ratio 45dB
Image Response Ratio 30dB
IF Response Ratio 60dB
Antenna . . . . . Ferrite loopstick antenna

Miscellaneous

Power Requirements . . . . . AC 120V, 60Hz
Power Consumption . . . . . 400W (UL)
Dimensions . . . . . 519(W) x 180(H) x 460(D) mm
20-7/16(W) x 7-1/16(H) x 18-1/8(D) in
Weight (without package) . . . . . 19.2 kg (42 lb 5 oz)

Furnished Parts

Operating instructions 1
FM T-type antenna 1

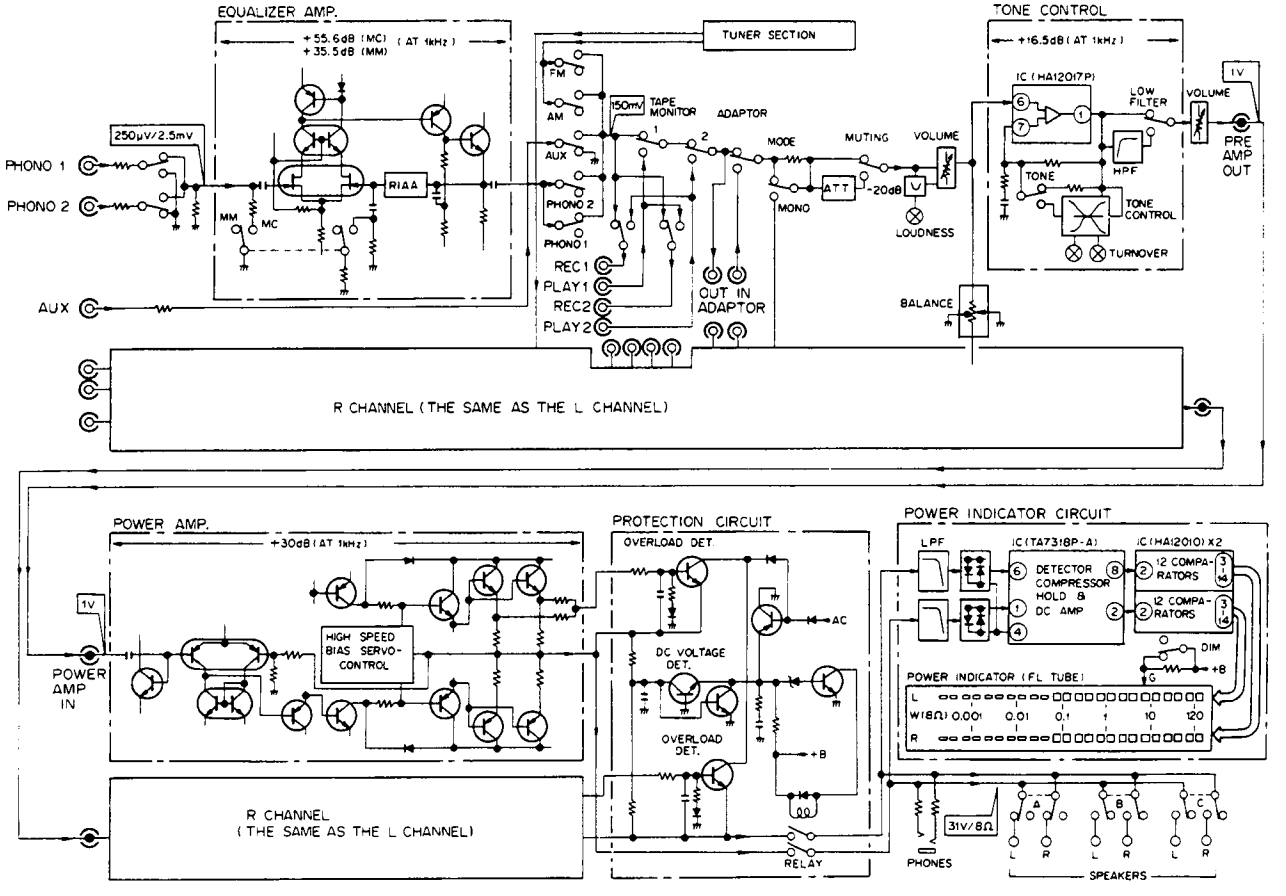
**Measured pursuant to the Federal Trade Commission's Trade Regulation rule on Power Output Claims for Amplifiers.*

NOTE:

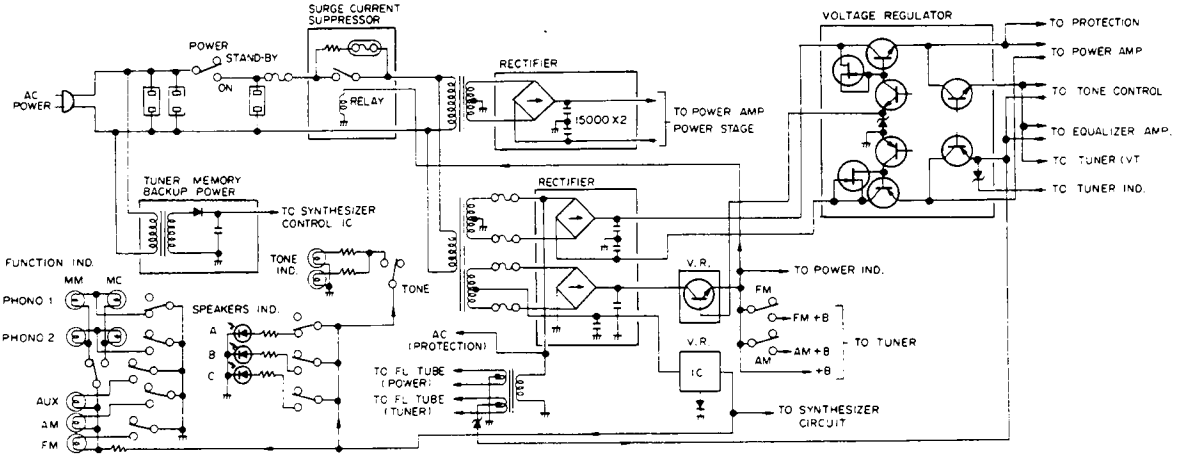
Specifications and the design subject to possible modifications without notice due to improvements.

3. BLOCK DIAGRAM

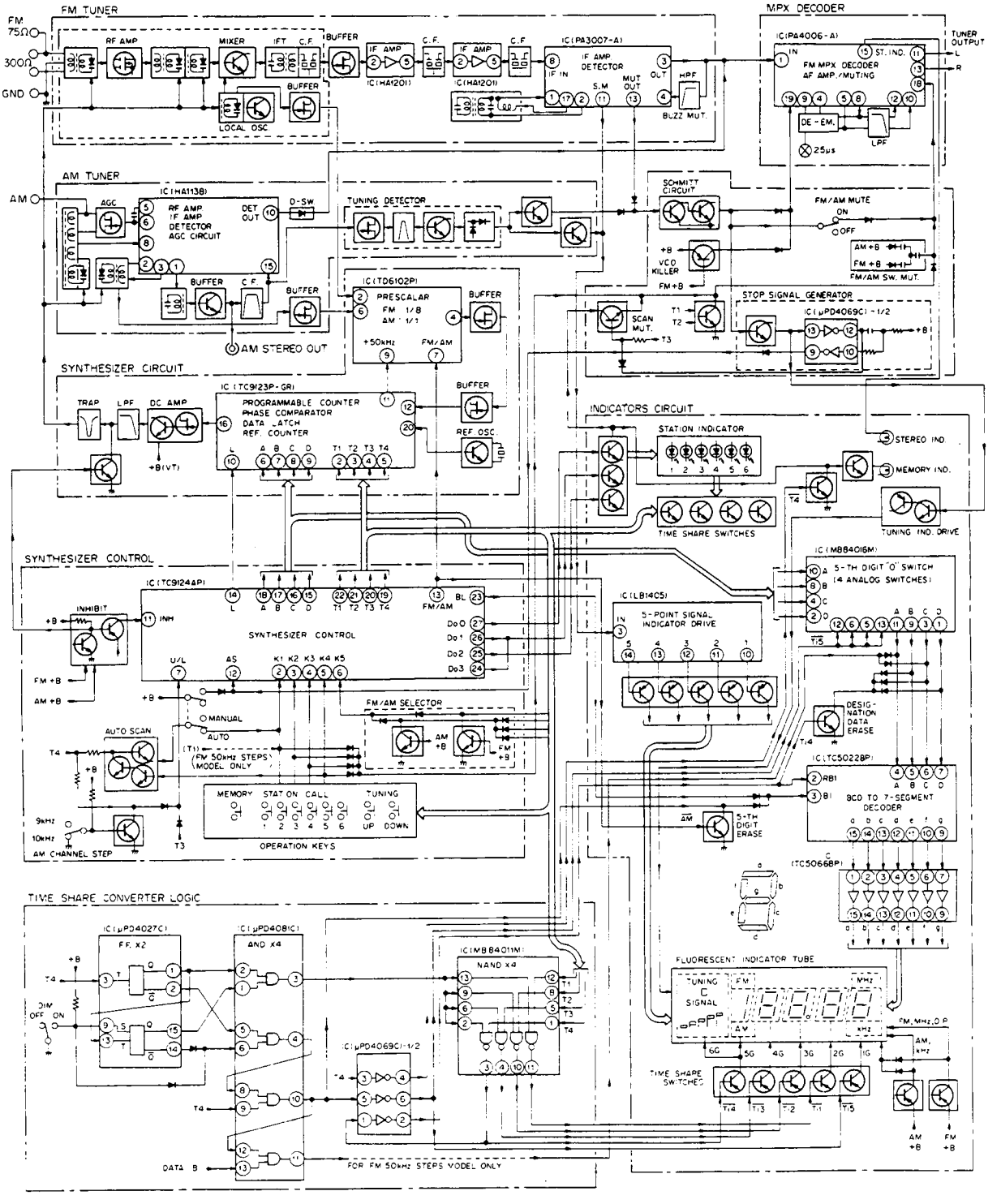
3.1 AUDIO SECTION



3.2 POWER SUPPLY SECTION



3.3 TUNER SECTION



4. CIRCUIT DESCRIPTIONS

4.1 MAJOR FUNCTIONS OF TUNER SECTION

The SX-D7000's tuner section is a crystal oscillator PLL Digital Synthesized Tuner. Major functions are enumerated briefly below.

1. Frequency Range

FM: 87.5MHz to 108MHz in 100kHz steps.

NOTE:
The SX-D7000/S/G model is 87.55MHz to 108MHz in 50kHz steps.

AM: 525kHz to 1605kHz in 1kHz steps (The auto scan tuning is stopped only at 10kHz integer multiples).

NOTE:
The SX-D7000 has been equipped with an AM CHANNEL STEP selector (10kHz/9kHz). When set in the 9kHz position, the 531kHz to 1602kHz frequency range is employed, and scan is stopped only at 9kHz integer multiples during auto scan tuning mode.

2. Tuning

- Frequency is changed by 1 step for every push operation of the TUNING UP and TUNING DOWN keys. (Each push operation changes the frequency by 100kHz in the FM band, and by 1kHz in the AM band).
- Frequency scanning is achieved by depressing the TUNING UP or TUNING DOWN key continuously.
- For auto scan tuning mode, set the tuning mode switch to the AUTO position and press either TUNING UP or TUNING DOWN key once. In this mode, the frequency band will be scanned automatically, coming to a stop when the frequency of a sufficiently strong broadcasting station (input level above a specific value) is tuned.
- Preselected tuning by memory read-out (preset frequency read out from memory for direct tuning).

3. Memory

- A total of 6 FM frequencies and 6 AM frequencies may be stored in the memory.
- Also auto memory of the previous tuned frequency when switching back and forth between FM and AM bands.
- Last-one memory (the last frequency tuned when the power is switched off will be automatically retuned when the power is switched back on).
- Memory maintained by a separate power supply when the main power is switched off (i.e. when the POWER switch is turned to STAND BY position).
- Memory also maintained (for 3 to 4 days) when the power is turned off completely (i.e. when power cord is disconnected or a power failure occurs).

4. Indicators

- The received frequency is displayed in digital form by fluorescent indicator tube.
- Signal strength is indicated by the SIGNAL indicator composed of fluorescent indicator tube 5-point indicator display.
- Tuning indicator.
- Memory read-out indicator.
- Memory write-in indicator.
- FM STEREO indicator.

4.2 FM TUNER SECTION

Front-End

The FM front-end includes a dual-gate MOS FET RF amplifier (single stage) and a variable capacitance diode corresponding to a 4-ganged tuning capacitor. The local oscillator signal is applied to the synthesizer circuit for comparison with a reference signal, the resultant tuning voltage then being applied to variable capacitance diode for determination of the oscillator frequency (i.e. tuning frequency).

IF Amplifier and Detector

These employ 3 ICs and 3 dual-element ceramic filters. The IC (HA1201) of the first 2 stage constitutes a single-stage differential amplifier current-limiting limiter. The IC (PA3007-A) in the third stage, an improvement on the former IF system IC (PA3001-A), includes an IF limiter amplifier, quadrature detector, meter drive, and other circuits. Performance in terms of distortion, S-N ratio, delay characteristics, and other parameters, shows a marked improvement in comparison to the PA3001-A.

Multiplex Decoder

The recently developed multiplex decoder IC (PA4006-A) combines MPX decoding with muting functions in a single IC, thereby handling the functions of the more conventional MPX IC (PA1001-A) and AF MUTING IC (PA1002-A).

Distortion ratings and S-N ratio have been further improved by incorporating a chopper type MPX decoder. The chopper type switching circuit operates by switching the signal either to ground or to the through circuit, thereby eliminating the generation of unwanted noise or distortion. Furthermore, since the PA4006-A features DC direct-

coupled switching with the detector, there is no deterioration in separation at the low frequency end.

Besides the decoder and muting circuits, the PA4006-A also incorporates the pilot signal conceller, stereo auto selector, VCO killer circuit, muting amplifier, and muting control circuit.

De-emphasis involves the use of the audio amplifier NFB circuit, while the muting gate is opened and closed according to the various muting signals from the internal control circuit and other external circuits.

4.3 AM TUNER SECTION

See Fig. 4-1 for an outline of the AM tuner IC (HA1138). The tuning circuit employs a variable capacitance diode (vari-cap) which corresponds to a 2-ganged tuning capacitor. The local oscillator signal is compared with a reference signal in the synthesizer circuit, and the resultant tuning frequency then applied to the vari-cap for determination of the oscillator frequency (tuning frequency). And in order to improve performance with strong input signals, the IC has been equipped with an AGC (automatic gain control) circuit, and the bar-antenna fitted with a damping coil. The AGC varies the damping current by means of an FET according to the RF amplifier output level.

The AM STEREO OUT terminal on the rear panel is for connecting to an AM stereo broadcast decoder adaptor. The signal appearing at this terminal is the mixer output passed via a buffer (emitter-follower) stage.

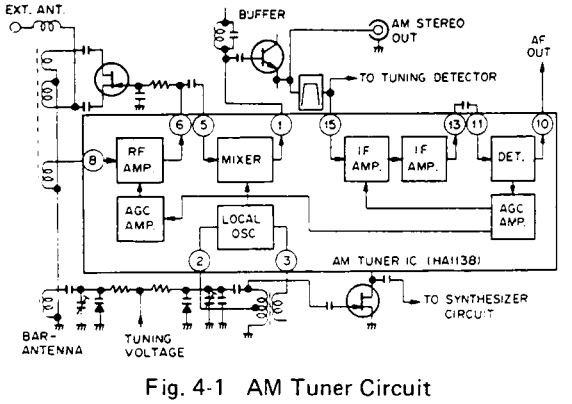


Fig. 4-1 AM Tuner Circuit

4.4 SYNTHESIZER CIRCUIT

Outline of Basic Operating Principles

An outline of the basic composition of the PLL digital synthesizer circuit is shown in Fig. 4-2. Although the actual circuit also includes a high speed scaling circuit because of the restrictions imposed by IC operational frequency limits, the basic principles are the same, and the circuit has therefore been omitted.

The output signal fs of the voltage controlled local oscillator (VCO) undergoes 1/N frequency division in the programmable counter, followed by phase comparison with the output signal fr from the crystal controlled reference oscillator. The output from the phase comparator is then passed through a loop filter to become a DC voltage Vd which in turn controls the VCO. And since fs/N equals to fr in this closed loop, the VCO output frequency will be N times the reference frequency where N is an integer. Since the programmable counter varies the frequency division numerator N according to program signal, the VCO output frequency fs (local oscillator frequency) will be determined according to the program signal, becoming N times (integer multiple) the reference frequency fr.

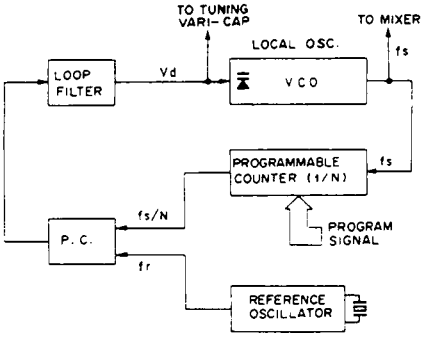


Fig. 4-2 Basic Composition of the PLL Synthesizer Circuit

Synthesizer Circuit in the SX-D7000

The composition of the synthesizer circuit employed in the SX-D7000 is outlined in Fig. 4-3. The major component in this circuit is the TC9123P-GR C MOS IC. Because of the restrictions imposed by the operational frequency limits of this IC, the frequency of the local oscillator during FM reception is divided by 8 in the ECL (emitter-coupled logic) prescalar IC (TD6102P) prior to being applied to the TC9123P-GR IC.

The data program signals used to designate FM/AM operation and the programmable counter frequency division ratio consists of BCD code pulse (A—D), time division pulse (T1—T4), and load

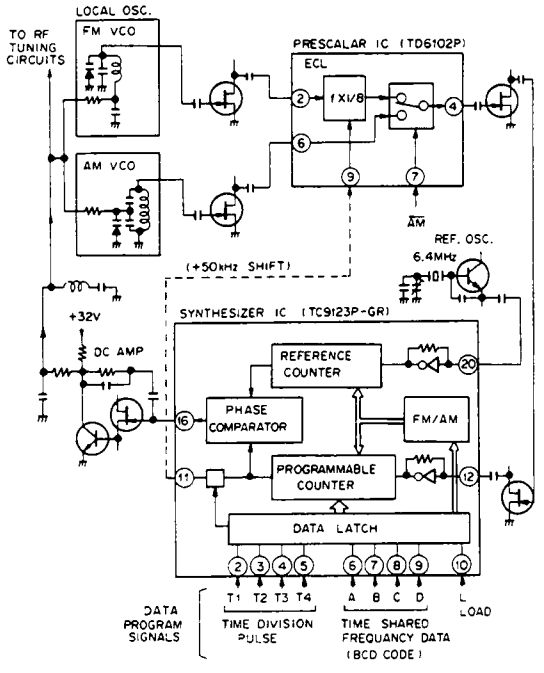


Fig. 4-3 SX-D7000 Synthesizer Circuit

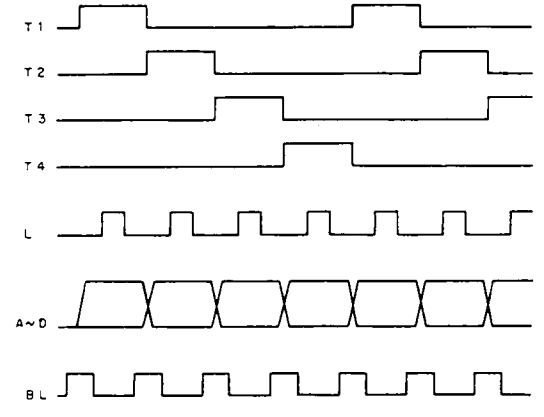


Fig. 4-4 Data Program Signal Time Chart

pulse (L) signals. See Fig. 4-4 for an outline of the data program signal time chart.

Numbers 0 to 9 are applied in BCD (Binary coded decimal) code to the synthesizer IC (TC9123P-GR) A—D inputs according to the T1—T4 timing. The unit digit of the reception frequency is applied at time T1, the ten digit at time T2, the hundred digit at T3, and the thousand digit at T4. This time shared data is then assembled by the latch circuit to form the frequency division ratio data. And since the thousand digit will not involve any number except 1, frequency data is applied only to input A at time T4, the B, C and D inputs serving as for data designating the FM/AM operational mode. Input L is the load pulse input employed to prevent mis-reading of input data. Data latching starts with down stroke of the load pulse.

The SX-D7000 synthesizer system is operated on the basis of time division pulses (T1—T4) prepared by the synthesizer control IC (TC9124AP). Data transfer is based on dynamic time division.

Operating During FM Reception

Fig. 4-5 outlines the block diagram of the SX-D7000 synthesizer stage during FM reception. With the basic operational step at 100kHz in Fig. 4-5, and the prescalar dividing the frequency by 8, the phase comparison frequency will be 12.5kHz. The reference frequency signal is obtained by dividing the 6.4MHz crystal oscillator output by 512. And since the reception band is 87.5MHz to 108MHz and the IF 10.7MHz, the local oscillator frequency will range from 98.2MHz to 118.7MHz. After dividing by 8 in the prescalar, this range will be 12.275MHz to 14.8375MHz. Hence, the 12.5kHz may be obtained by setting the programmable counter frequency division ratio N to 982 — 1187 for comparison with the reference signal in the phase comparator. The phase comparator output is passed via a low-pass filter to the tuning circuit vari-cap, resulting in the local oscillator frequency being locked to 8N times the reference frequency (12.5kHz), or in other words, N times 100kHz.

Since the reception frequency data (n) applied to the synthesizer IC (TC9123P-GR) is shown in the FL indicator tube (frequency display) as 875 — 1080, the required frequency division ratio may be obtained from the reception frequency data by programming for frequency division ratio N=n+107 during FM reception.

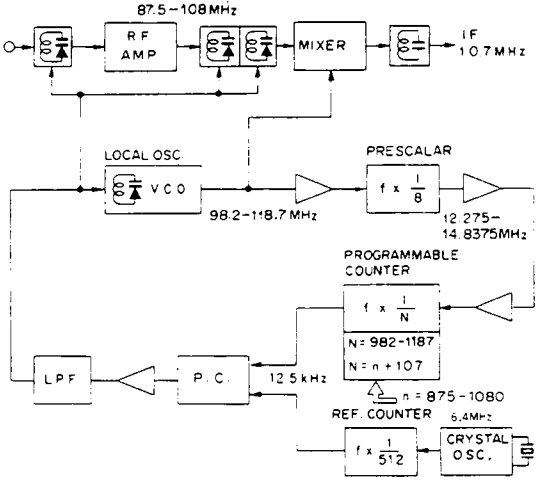


Fig. 4-5 Outline During FM Reception

- **50kHz Step Operation (Model SX-D7000/S/G)**

The circuit shown in Fig. 4-5 will only change the reception frequency in 100kHz steps unless otherwise modified. By altering the frequency division ratio N, a 50kHz shift circuit may be activated with every second 100kHz frequency shift, resulting in the reception frequency being changed in 50kHz steps.

The Fig. 4-5 circuit forms a PLL (phase locked loop) where the local oscillator signal is sampled, divided, and then locked to a frequency 8N times the reference frequency (12.5kHz). Consequently, any attempt to vary the local oscillator frequency will result in the voltage applied to the vari-cap being changed in a way that will tend to cancel this variation. If then by some means a count can be obtained 50kHz lower than the actual frequency when the local oscillator is being sampled, it will be possible to alter the voltage applied to the vari-cap so that the oscillation frequency is increased by 50kHz.

The prescalar IC (TD6102P) shown in Fig. 4-6 contains 3 separate 1/2 frequency dividers for a total frequency division of 1/8. If a single shift pulse is applied to pin 9, a pulse count at the 1/4 division stage will be eliminated. And if the shift pulse frequency is 12.5kHz, a total of 12,500 pulses will not be counted during the 1 second period. In terms of the IC input terminal (pin 2), this is equivalent to not counting 50,000 pulses within the same period, which in turn is equivalent to applying an input frequency which is 50kHz lower than the actual input frequency. The PLL consequently attempts to cancel this change, thereby increasing the voltage applied to the vari-cap so that the oscillation frequency is increased by 50kHz. The local oscillator frequency is thus locked at a frequency increased by 50kHz, thereby shifting the reception frequency by +50kHz.

The TC9123P-GR synthesizer IC has been designed to produce a 12.5kHz output signal (comparator signal) at pin 11 with every second step. By connecting this signal to pin 9 of the prescalar IC (TD6102P), input frequencies may be received in 50kHz steps.

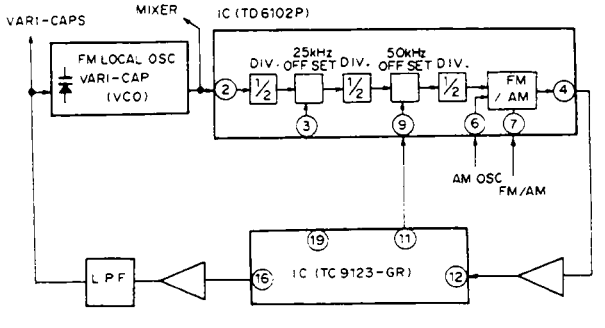


Fig. 4-6 50kHz Shift Circuit

Operation During AM Reception

Fig. 4-7 is a block diagram of the relevant parts of the synthesizer circuit involved in the reception of AM frequencies. With the reception band covering the 525kHz to 1605kHz range, and the IF signal set to 460kHz, the prescalar circuit is not required. Since frequencies are shifted in 1kHz steps, the phase comparator frequency will be 1kHz. The reference signal is obtained by dividing the crystal oscillator frequency (6.4MHz) by 6400. With the local oscillator frequency ranging from 985kHz to 2065kHz, 1kHz is achieved by setting the programmable counter frequency division ratio to the 985 to 2065 range, and this is compared with the reference signal in the phase comparator. The output of this comparator is then applied to the tuning circuit vari-cap via a low-pass filter, resulting in the local oscillator frequency being locked to N times the reference frequency (1kHz).

Again, since the reception frequency data (n) applied to the synthesizer IC (TC9123P-GR) is shown in the FL indicator tube (frequency display) as 525 — 1605, the required frequency division ratio may be obtained from this reception frequency data by programming the frequency division ratio as N=n+460 during AM reception.

NOTE:
The SX-D7000 has been designed with an AM CHANNEL STEP selector (10kHz/9kHz). When switched to the 9kHz position, the reception band becomes 531kHz — 1602kHz, the IF signal 459kHz, and the programmable counter frequency division ratio N=n+459=990—2061.

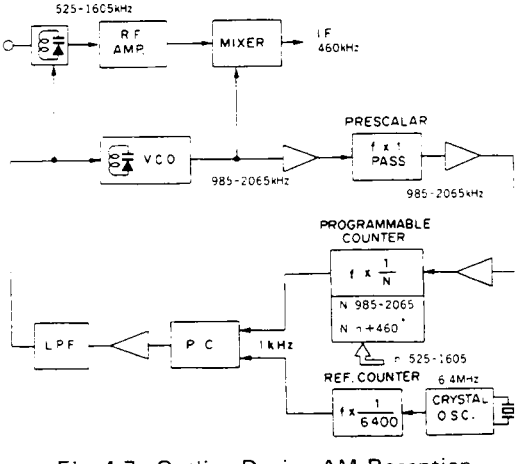


Fig. 4-7 Outline During AM Reception

4.5 SYNTHESIZER SYSTEM CONTROL CIRCUIT

The synthesizer control IC (TC9124AP) is an extremely complex IC, so the block diagram shown in Fig. 4-8 includes only the more important components. The IC input and output terminals are briefly described below.

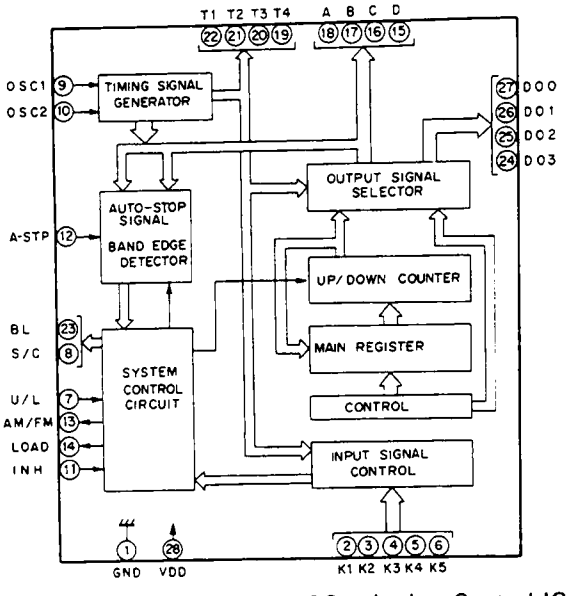


Fig. 4-8 Block Diagram of Synthesizer Control IC

Time Division Pulse Terminals (T1–T4)

The time division pulse generated by TC9124AP (outlined in Fig. 4-4) is a time-sharing timing signal used in synchronizing almost all TC9124AP inputs and outputs.

Table 1 Decimal Numbers and BCD Code

Decimal Numbers	8-4-2-1 Code (BCD)
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1

Table 2 Reception Frequency Data

Data	T1		T2		T3		T4	
A	Frequency data unit digit	1	Ten digit	10	Hundred digit	100	1000	.....
B		2		20		200	Reception mode Designation	
C		4		40		400		
D		8		80		800		

Reception Frequency Data Terminals (A–D)

The A–D terminals are employed in the transfer of reception frequency data in BCD code, and are synchronized with the time division pulse. The reception frequency data is handled in BCD code by the A–D terminals during the T1–T3 timing, and by the A terminal during the T4 timing (see Table 2). Furthermore, during the T4 timing, the B, C and D terminals are utilized in designating the operational mode of the synthesizer IC (TC9123P-GR) as shown in Table 3. The SX-D7000/KU model employs AM1 or AM2 (switchable) and FMU.

NOTE:
The SX-D7000/S/G model operates in AM1 or AM2 (switchable) and FME.

Input Terminals (K1–K5)

K1–K5 handle the different command inputs according to the operation key input and the relevant T1–T4 timing.

- **Operation Designation**

A K5 input determined according to T2 timing corresponds to FM mode, while a similar input determined according to T1 timing corresponds to AM mode. By applying an input to U/L according to T3 timing, the FM reception band is switched to FMU (87.5–108MHz). By applying an input to U/L according to T4 timing, the AM reception band is switched to AM1. Unless otherwise specified, AM reception is in AM2 mode.

NOTE:
The SX-D7000/S/G model is designed for FME mode operation (input applied to K1 terminal according to T1 timing).

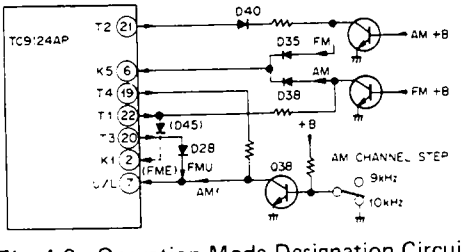


Fig. 4-9 Operation Mode Designation Circuit

Table 3 Operation Designation Data

Mode	B	C	D	Remarks
FMU	1	1	1	FM 87.5–108MHz
FME	(0 or 1)	1	1	FM Europe: 50kHz steps
FML	1	0	1	FM 76–90MHz
AM1	0	1	0	AM inter-station steps: 10kHz
AM2	0	0	0	AM inter-station steps: 9kHz

- Manual Tuning

With an input applied to K4 according to T3 timing for a short period of time, the reception frequency is shifted downwards in steps of 100kHz during FM mode, and 1kHz during AM mode. If the input is applied longer than a specified length of time, the down shift will proceed at a rapid rate, coming to a stop only when the input is stopped. Likewise, when an input is applied to K4 according to T4 timing, the reception frequency is shifted upwards (see Fig. 4-10). Note that during manual tuning, the reception frequency shift will stop when either the upper or lower band edge is reached.

- Auto Scan Tuning

The auto scan tuning mode is activated when an input is applied to K1 according to T2 timing.

When the AUTO/MANUAL switch (in Fig. 4-10) is set to the AUTO position, the emitter of Q26 is connected to K1. If Q25 has been turned off with the base of Q26 connected to T2, Q26 will subsequently turn on and off synthronized by T2. When either the UP or DOWN key is pressed, T3 or T4 will charge up C113 via D30 resulting in Q24 being turned on once the base voltage has reached a certain value. Q25 will consequently be turned off, and Q26 will operate according to T2 synchronization. An input synchronized by T2 will then be applied to K1, resulting in the start of the reception frequency scanning. This scanning action will commence almost as soon as either the UP or DOWN key is pressed, and will continue after the key is released. If either band edge is reached, the reception frequency scanning will not stop, but proceed in the reverse direction.

The scanning will stop as soon as the AS terminal of the IC is switched to high level. If there is no muting signal, a stop pulse will be applied to the AS terminal to stop the scanning. The generation of the stop pulse is described later under section "Auto Scan Stop Circuit".

Since there is no means for detecting the carrier frequency during the reception of AM broadcasts, the auto scanning operation would be likely to stop 1 or 2kHz prior to the actual central frequency when the input signal is very strong. So in order to avoid this, the auto scan mode has been programmed to stop only at frequencies which are integer multiples of 10kHz (AM1 mode) or 9kHz (AM2 mode).

- Preset Tuning

The SX-D7000 can store up to 6 FM frequencies and 6 AM frequencies in its memory.

When an input is applied to K2 according to T2 timing (MEMORY key), and then an input applied to K1—K3 according to T3 and T4 timing within a prescribed length of time (3 seconds) (STATION CALL key), the tuned frequency will be stored in one of the memories (1) to (6) (see Fig. 4-11 and Table 4). And by switching between AM and FM bands (an input applied to K5 according T3 and T4 timing), frequencies may also be stored in memories (7) to (12).

Then when a STATION CALL key (1—6) only is pressed, the frequency data stored in the corresponding memory may be retrieved for immediate tuning to that frequency.

Table 4 Memory Designations

	T3	T4	T2
K1	Memory (1)	Memory (2)	.....
K2	(3)	(4)	Memory write-in
K3	(5)	(6)	.....
K5	(1, 3, 5) + 6	(2, 4, 6) + 6	.....

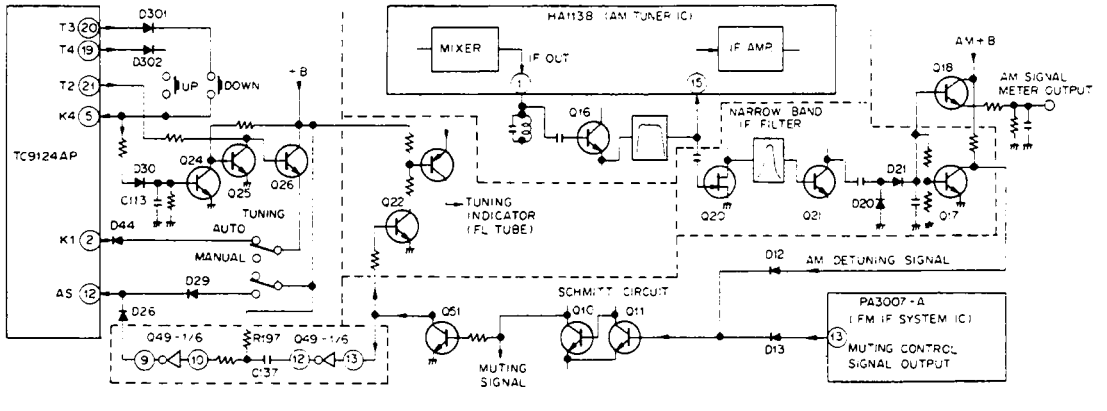


Fig. 4-10 Auto Scan Control Circuit

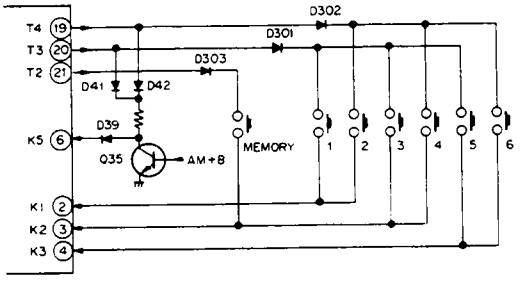


Fig. 4-11 Memory Write-in Circuit

Auto Scan Stop Circuit (Fig. 4-10)

- AM Tuning Detector

This circuit detects the auto scan stop data signal during AM reception. The tuning condition is detected by applying the AM IF signal to a narrow band filter and then amplifying and rectifying the signal. The rectified output is inverted by Q17, and AM tuning detector output is switched to low level when the frequency is tuned. The rectified output is also passed via Q18 to become the AM tuner signal meter drive output.

NOTE:
Although accurate tuning cannot be detected by this circuit alone, the mechanism by which the auto scan tuning mode is stopped only at frequencies which are 10kHz or 9kHz (switchable by AM CHANNEL STEP selector) integer multiples does enable accurate tuning.

- FM Tuning Detector

When the input level is very weak, or when tuning away from a station, a DC voltage appears at pin 13 of the FM IF system IC (PA3007-A). This output signal is switched to low level when the frequency is tuned.

- Stop Pulse Generation

The auto-stop pulse is used to halt the auto scan mode. The low level output of FM tuning detector corresponds to correct tuning during FM reception, and during AM reception. Furthermore, the low level output of AM tuning detector corresponds to tuned status during AM reception, and during FM reception. Consequently, when a frequency is tuned during either AM or FM reception, the Schmitt circuit (Q10, Q11) output is switched to low level. As a result, Q51 is turned off, and collector voltage increased. This voltage is then inverted by inverter Q49 (13-12), and differentiated by C137/R197 in order to detect the voltage change. The resultant voltage is inverted by inverter Q49 (10-9), and then applied via D26 to the AS terminal of TC9124AP as a positive pulse (detected when Q51 is turned off). The auto scan mode is thus brought to a stop.

If the AUTO/MANUAL selector is set to the MANUAL position, the AS terminal is switched to high level via D29, thereby preventing commencement of the auto scan operation.

Auto Memory

When switching back and forth between FM and AM bands, the reception frequency data (in the main register) is automatically transferred to the sub register, and the contents of the sub register automatically transferred to the main register (i.e. exchange of data). This operation is program controlled. Consequently, whenever the FUNCTION (FM or AM) key is switched over, the formerly tuned frequency is retuned automatically, thereby eliminating the need to repeat tuning procedures again for that station.

Memory Holding

When the synthesizer control IC (TC9124AP) INH terminal is switched to low level, an inhibit function is activated. The complete supply of operation clock signals within the IC is consequently stopped, thereby putting the IC into a complete static condition, and this condition is maintained as long as the inhibition is applied—there being no inputs or outputs handled whatsoever, even when any of the operation keys is pressed. Since this is a CMOS IC, the power consumption during inhibition mode is extremely small (measured in microamps).

The TC9124AP power supply is backed by the subsidiary power supply circuit, and this maintains the TC9124AP power supply even after the power switch has been turned off (STAND BY position). In this case, if the AM+B and FM+B supplies are stopped, the memories will be maintained under inhibit mode. Furthermore, if the AC line supply is disconnected altogether, the memories will still be maintained (about 3 days) by means of a large capacitance capacitor (C2).

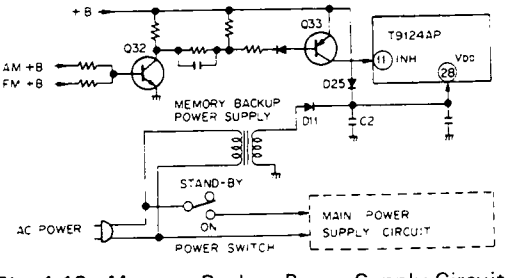


Fig. 4-12 Memory Backup Power Supply Circuit

4.6 DISPLAY CIRCUIT OF THE TUNER SECTION

Frequency Display

The SX-D7000 displays the selected station frequency on a 5-digit digital display using a fluorescent indicator tube (FL tube) as a source. As noted in Fig. 4-13, the FL tube display grids are divided into five independent units. Drive is by the dynamic time division method; a time cycle is divided into five divisions, and each digit pulsates in a recurring sequence. The flicker inherent in this method is not detectable by the human eye.

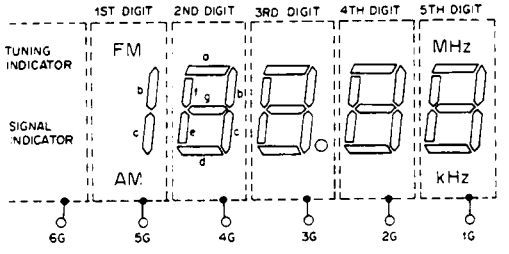


Fig. 4-13 FL Tube 5-digit Digital Display

- **Time-share Converter Logic**

The SX-7000 synthesizer system divides a time cycle into four parts (T1 — T4) and uses pulse trains to transfer data. The synthesizer control IC TC9124AP outputs the BCD coded selected station frequency from terminals A, B, C and D as time-shared reception data, and transfers it on the clock pulses of T1 thru T4. (See Table 2) In order for this 4-part time-shared reception data to appear on a 5-digit display, the time-share converter logic must convert the 4-part pulse signal (T1 — T4) to a 5-part pulse signal (Ti1 — Ti5).

This circuit also functions to control the brightness of the FL tube display through the dimmer switch.

NOTE:

The selected station frequency in the FM mode moves up or down the spectrum in 100kHz steps in the SX-D7000/KU model, and thus could be displayed using a 4-digit display, however the step change in the SX-D7000/S/G model is 50kHz, necessitating a 5-digit display. The same circuit is used in both models, consequently the 5th digit on the SX-D7000/KU model is always "0".

In the AM mode, the selected station frequency changes in 1kHz steps and is displayed with four digits; the 5th digit being extinguished during this mode.

Fig. 4-14 illustrates the configuration of the timeshare converter logic. The terminals 1G thru 6G noted on the right side of the figure are connected to the FL tube grids (See Fig. 4-13). When no time division pulses (T1 — T4) are present, the NAND gates 1 thru 4 (Q47) and the NOT gate (Q49) output P, O, R, S, and U respectively at a high level. Thus, Q5 thru Q9 are off; the FL tube grids are reverse-biased, and no light is emitted.

Fig. 4-15 shows the time division pulse time chart. When the dimmer switch is in the OFF position, the time division pulses U, S, R, Q, and P shown in Fig. 4-15 are applied to the bases of Q5 thru Q9. One by one they become active, providing dynamic time division drive to the 5-digit display. When the dimmer switch is in the ON position, time division pulses U', S', R', Q', and P' are applied to the bases of Q5 thru Q9. The frequency of occurance of these pulses is only one half of those occurring when the dimmer switch is in the OFF position, bringing the intensity of illumination of the FL tube down proportionally.

Referring to Fig. 4-14, when the dimmer switch is in the OFF position and pulse T4 (Fig. 4-15-T4) is applied to the clock terminal (T) of flip-flop 1 (Q46), the output E is as illustrated in Fig. 4-15-E. (Flip-flop 1 is reversed on the rising edge of T4, and divides the frequency of the pulse in half.) When a +B signal applied to the set terminal (S) of flip-flop 2 brings it to a high level, output G from the Q terminal goes to high level independent of the input at the clock terminal (T). Output M from AND1 (Q48) is gated by input G at a high level, and is equal to input E. It is illustrated by Fig. 4-15-E. AND2 (Q48) will gate when D52 is conducting, thereby setting input H to a high level. Output N is equal to input F, and is illustrated by Fig. 4-15-F. Output J from AND3 (Q48) is the AND of input N (Fig. 4-15-F) and T4 and is illustrated by Fig. 4-15-J. The output P, Q, R, and S of NAND1 thru 4 (Q47) is the AND negation of input M (Fig. 4-15-E) and T1 thru T4, and is illustrated by Fig. 4-15-P, Q, R, S. Output U from NOT (Q49) is the negation of input J (Fig. 4-15-J) and is shown by Fig. 4-15-U.

In Fig. 4-14, output E of flip-flop 1 is the same regardless of whether the dimmer switch is in the ON or OFF position (Fig. 4-15-E). When the set terminal of flip-flop 2 is at a low level, the input pulse to the clock terminal is halved in frequency. The input to the clock terminal is illustrated in Fig. 4-15-E. Output G from the Q terminal becomes as is illustrated in Fig. 4-15-G'. Output M from AND1 (Q48) is the AND of input E and G and is noted by Fig. 4-15-M'. Output N from AND2 (Q48) is the AND of input F (Fig. 4-15-F)

and H (Fig. 4-15-H') and is illustrated by Fig. 4-15-N'. Output J from AND3 (Q48) is the AND of input N (Fig. 4-15-N') and T4, and becomes Fig. 4-15-J'. NAND1 thru 4 (Q47) outputs P, Q, R, and S. These are the negative AND of input M (Fig. 4-15-M') and T1 thru T4 and are illustrated by Fig. 4-15-P', Q', R', and S'. Output U of NOT (Q49) is the negation of input J (Fig. 4-15-J') and is shown by Fig. 4-15-U'.

Through the use of the above logic gates the indicator time division pulses (Ti1 — Ti5) are synchronized with T1 thru T4, and provide for the display of the time-shared reception data (selected station frequency data) by the 1st through 4th digit of the FL tube. The time division pulse (Ti5) for the 5th digit is actually synchronized with T4, however, at this time the selected station frequency data is blocked out and substitute data is displayed by the 5th digit. This will be described later.

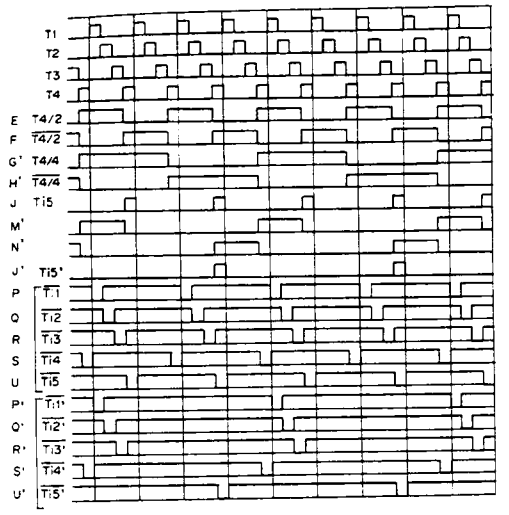


Fig. 4-15 Time Division Pulse Time Chart

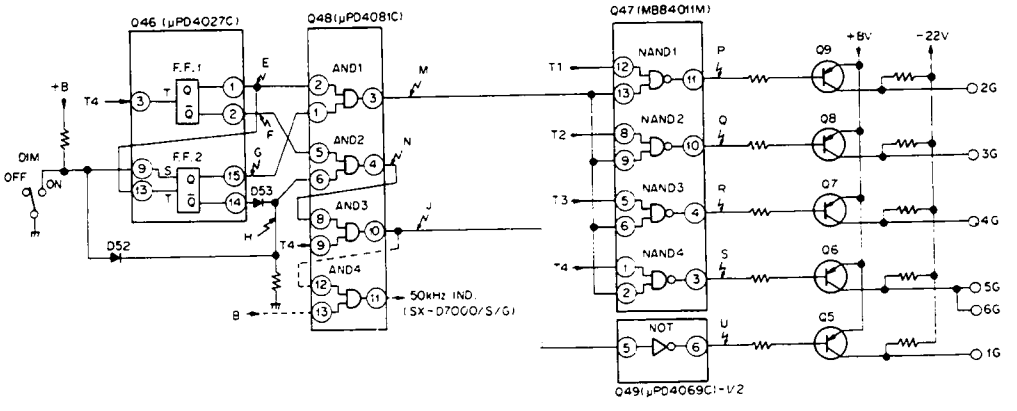


Fig. 4-14 Time-share Converter Logic Circuit

- **Anodes of the FL Tube Drive Circuit**

The formulation of the numerical digits by the FL tube is accomplished by 7 segments, illustrated as a through g in Fig. 4-13. (The first digit uses only b and c.) TC9124AP transmits the time-shared reception frequency data T1 — T4 as BCD code from terminals A, B, C, and D. (See Table 2.) MB84016M (Q40) in Fig. 4-16 is an electronic switching device activated by the appearance of a $\overline{Ti5}$ pulse, as represented by U and U' in Fig. 4-15. It serves to inhibit the transmission of frequency data to the 5th digit. The frequency data is converted from BCD code to decimal number 7-segment display data by TC5022BP. The 7-segment display data is passed through TC5066BP (non-inverting buffer IC) and applied to the anode segments (a thru g) of the FL tube. Each digit shares the segments a thru g connected in parallel, and each digit's independent grid is sequentially scanned by the pulses Ti1 — Ti5, displaying the selected station frequency in a rapidly flickering display.

The B, C, and D data passed on the T4 pulse is not actually frequency data (it is operation designation data to TC9123P-GR). Q45 conducts with the appearance of T4, passing B, C, and D to ground via D49 — D51, and thus avoiding unnecessary data being sent to TC5022BP.

The BL terminal of TC9124AP outputs a display blanking signal (Fig. 4-4) during the period the time division pulses (T1 — T4) are in transition. When this is applied to the BI terminal of TC5022BP, the output (a — g) of TC5022BP goes low level regardless of the level of input (A, B, C, D), thus preventing the blurring when transition is made from one display digit to another.

With the appearance of Ti5, Q40 goes non-conducting bringing the 5th digit data A, B, C, and D all to a low level. This input state has the same meaning as zero frequency data to TC5022BP, thus a "0" is displayed as the 5th digit on the FL tube. (During FM reception.)

The FM/AM converter signal (low level during AM reception) to the prescaler IC is applied to the base of Q50, therefore Q50 is non-conducting during AM reception. Thus with the transit of Ti5, the BI terminal (display blanking) of TC5022BP goes to a high level, and all outputs (a — g) are low level, extinguishing the 5th digit display during AM reception.

- **50kHz Step Indication (SX-D7000/S/G only)**

The operation designation data for FM reception for SX-D7000/S/G is FME. (See Table 3.) During the FME mode, if data B is "1" (high level) with the transit of T4, +50kHz shift operation is performed. Thus, when data B is at a high level with the transit of Ti5, the 5th digit of the FL tube displays a "5".

Q40 goes off with the appearance of Ti5. If at this time data B is at a high level, A and C, input to TC5022BP via D46 and D47 will go high level. This input state (A and C high level, B and D low level) mean a frequency data of "5", thus the 5th digit of the FL tube displays a "5".

- **Elimination of 1st digit**

Since there are 5 digits in the frequency display, the 1st digit will be "0" for any frequency under AM 1000kHz and FM 100.00MHz. In order to eliminate this zero (which in fact would turn out to be a "1" since the 1st digit only contains b and c segments), Ti4 is applied to the RBI terminal of TC5022BP.

The 1st digit would be set to 0 when A is switched to low level, but set to 1 when A is switched to high level according to T4 timing. And since Q45 is turned on at Ti4 timing, B, C and D are switched to low level. The RBI terminal input (Ti4) is inverted by NOT1 to low level. So if A is switched to low level at T4 timing, the NAND2 inputs will both become low level, and the output high level. The OR3 output will thus be switched to high level, resulting in all TC5022BP outputs being switched to low level. Hence, there will be no zero display at the 1st digit.

Station Memory Display

D01 — D03 of TC9124AP obtain the memory (1 — 12) call indicator output according to T1 — T4 timing (see Table 5). Since the SX-D7000 stores up to 6 AM frequencies (in memories 1 — 6) and FM frequencies (in memories 7 — 12), and indicates these by means of 6 indicator lamps (LED), memories n and n+6 (n: 1 — 6) will be shown by the same LED indicator (see Fig. 4-17).

The memory write-in display output is obtained from D00 according to T4 timing. When the MEMORY key is pressed and the MEMORY indicator lamp lights up, data may be written into the memory. If a STATION CALL key is then pressed during this condition the tuning frequency will be stored in the memory, and the MEMORY indicator lamp subsequently turned off. If none of the STATION CALL keys is pressed within 3 to 4 seconds, the write-in enable status will be released and the MEMORY indicator lamp turns off.

Signal Indicator

The SX-D7000 signal meter is an FL tube 5-point display driven by the meter drive IC (LB1405) (see Fig. 4-18). The signal meter drive signals from the FM and AM tuner sections are applied to a set of 5 voltage comparators which are activated according to the difference between the applied signal level and respective reference voltage levels allotted to each comparator. Q10 — Q14 are thus turned on according to a priority basis, resulting in the corresponding signal indication segment of the FL tube light up.

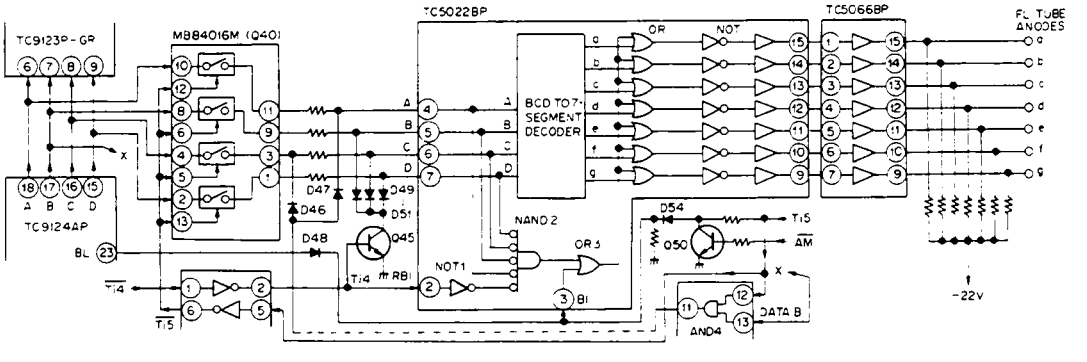


Fig. 4-16 Anodes of the FL Tube Drive Circuit

4.7 AUDIO SECTION

Phono Equalizer Amplifier

Fig. 4-19 shows the basic circuit of the equalizer amplifier. The first stage is a differential amplifier consisting of a ultra-low-noise twin FET and NPN twin transistor connected in cascade, the load circuit of which is a current mirror circuit.

The cascade connection serves to reduce the load impedance of the FET. This prevents deterioration in high-frequency response due to Miller Effect, and also reduce gate leak current noise on account of the reduced drain-to-source voltage. High voltage gain is provided in the following stage by a bootstrap circuit. The output impedance lowered using an emitter follower at output stage.

The input sensitivity and input impedance are selected by the PHONO MM/MC switch. In the MC position, an input sensitivity 10 times greater than that in the MM position, is obtained by reducing the amount of NFB.

Table 5 Memory Display

	T1	T2	T3	T4
D01	Memory (1)	Memory (2)	Memory (3)	Memory (4)
D02	(5)	(6)	(11)	(12)
D03	(7)	(8)	(9)	(10)

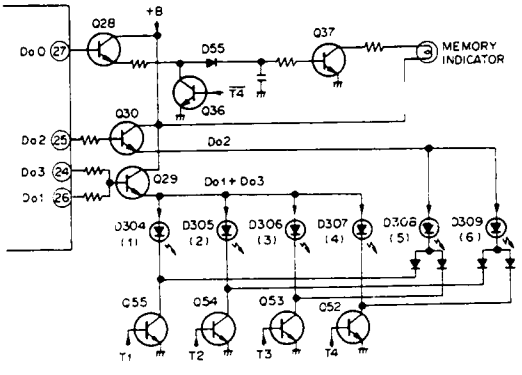


Fig. 4-17 Station Memory Display Circuit

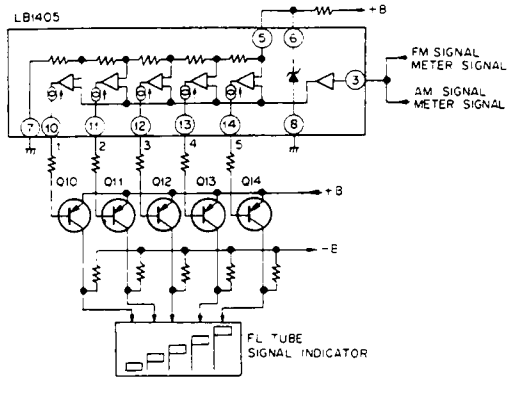


Fig. 4-18 Signal Indicator Circuit

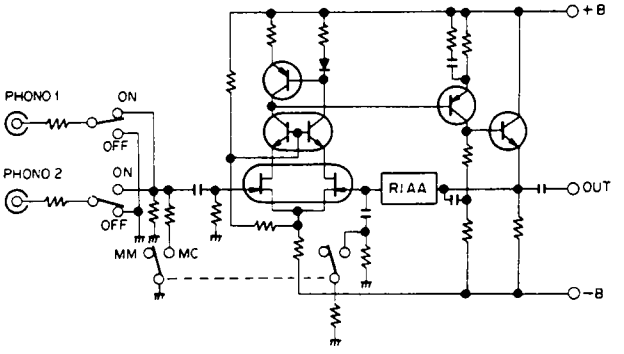


Fig. 4-19 Phono Equalizer Amplifier Circuit

Tone Control Circuit

Fig. 4-20 shows the basic configuration of the circuit. This circuit is an NFB type tone control with IC (HA12017P).

Tone control (BASS, TREBLE) is accomplished by providing the tone amplifier NFB circuit with a frequency selective characteristic. The capacitance of C1 — C4 are changed by TURNOVER switches (by adding another capacitors in parallel) to provide selection of the frequency.

The NFB circuit is changed to a flat frequency characteristic when the TONE switch in the OFF position.

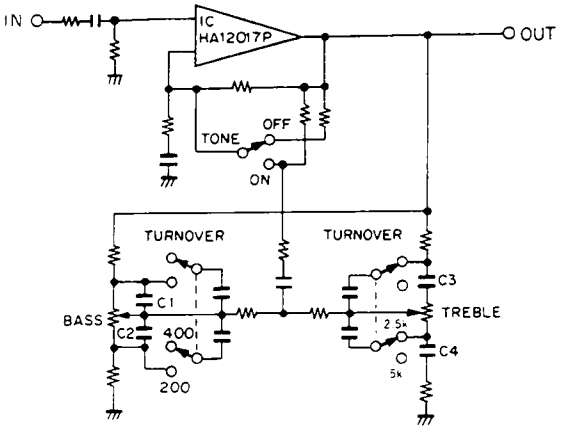


Fig. 4-20 Tone Control Circuit

Power Amplifier Section

- Amplifier Circuit

The basic circuit arrangement of the power amplifier is shown in Fig. 4-21. The first stage is a differential amplifier comprising PNP twin transistor (Q2), the load circuit of which is a current mirror employing an NPN twin transistor (Q3). The current mirror provides push-pull operation

in this stage, which serves to cancel even harmonics and further increase gain.

Q1 in the input circuit absorbs outflow of base current from Q2, and prevents the generation of a DC voltage. Because Q1 follows any temperature drift in Q2, temperature drift of the center point voltage is prevented.

The pre-driver stage (Q4, Q5) is a Darlington arrangement, the load circuit of which employs a constant-current source (Q6) resulting a high voltage gain.

The power stage bias voltage is supplied by the high speed bias servocontrol circuit. The high speed bias servocontrol circuit provides non-switching operation in the power stage (refer to "High Speed Bias Servocontrol Circuit).

The power stage (Q7 — Q12) is a 2-stage Darlington arrangement, the final stage is parallel SEPP circuit. Because there is no time constant in the NFB circuit in the low frequency region, amplification is possible down to DC (DC inputs will be cut off, by the input coupling capacitor).

- **High Speed Bias Servocontrol Circuit**

By operating the power stage only within the active region (no possible cut-off) and with minimum idle current, the high speed bias servocontrol circuit prevents the generation of switching distortion and reduces heat loss.

This circuit is outlined in Fig. 4-22. When there is no signal applied to the circuit, Q1 and Q2 are almost cut off, while Q3 and Q4 will be on. The voltage across the collector and base of both of these transistors (Q3 and Q4) at this time may be disregarded. Consequently, with the power stage bias circuit consisting of 4 PN junctions formed by Q3, D3 and Q4, and VR1.

With R1 and D1 ensuring a constant flow of current, the base of Q1 and point X may be brought to the same level on an AC basis (level fluctuations due to the signal) by a simple shift in DC level. Furthermore, Q1 may be considered

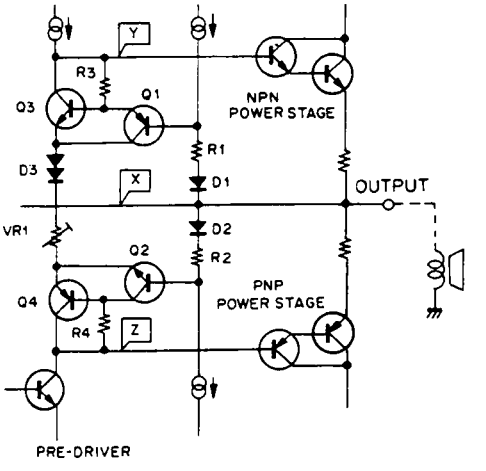


Fig. 4-22 Basic Circuitry of High Speed Bias Servocontrol Circuit

emitter-follower with R3 as the emitter resistance.

When the voltage across points Y and X is increased by the positive portion of the signal applied to this circuit, it becomes the input signal of this emitter-follower (Q1). Since the emitter-follower voltage gain is practically 1, a voltage more or less equal to that of the input signal (that is, the voltage increase across points Y and X) is produced at R3. And the R3 voltage is the voltage applied across the base and collector of Q3 which forms part of the power stage bias circuit. So the bias voltage applied to Q3 will be in excess by the same amount the voltage across points Y and X is increased (by positive portion of the signal) above the voltage level when no signal is being applied. Consequently, the increase in voltage across points Y and X cancels the decrease in voltage across points X and Z, thereby maintaining the idle current without cutting the PNP power stage off (noting that there actually is a slight decrease in current). For the negative portions of the signal, Q2 and Q4 are operated in the same manner, thereby preventing the NPN power stage form being cut off.

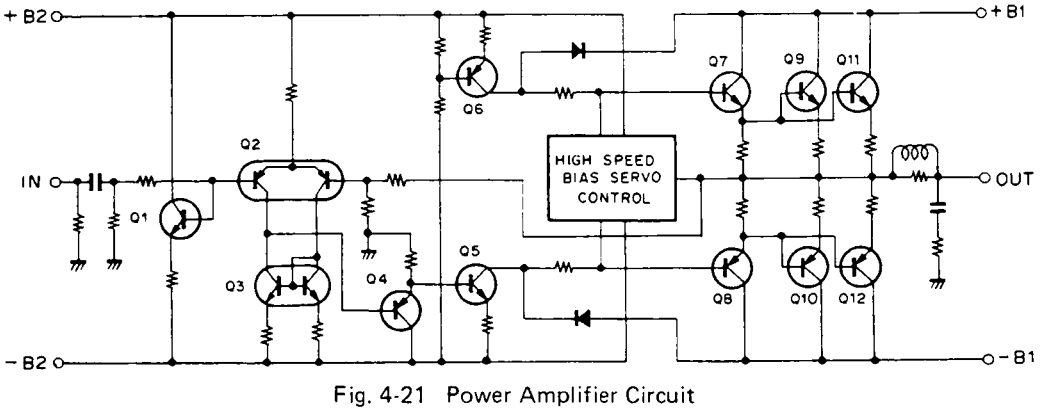


Fig. 4-21 Power Amplifier Circuit

4.8 POWER INDICATOR CIRCUIT

An outline of the output power indicator drive circuit is shown in Fig. 4-23. The output circuit signal is first passed through a low-pass filter and a compressor circuit before being applied to pin no.6 (4) of the IC (TA7318P-A). The compressor circuit makes use of the non-linearity of rising portion of the diode's Vd-Id characteristics to contract the signal dynamic range by 20dB. The IC contains a detector circuit, compressor (40dB), and peak hold circuit for both left and right channels. The dynamic range of the signal is thus contracted by 60dB to obtain a "peak held" DC voltage.

The output power indicator segments of the fluorescent indicator tube (FL tube) are driven by the HA12010 ICs (one for each channel) equipped with 12 pairs of voltage comparators. These comparators are biased at increasing levels, so each comparator will commence to operate separately as the input level increases. And since these comparators apply the voltages to the output power indicator segments, each successive segment will light up in turn as the input level rises.

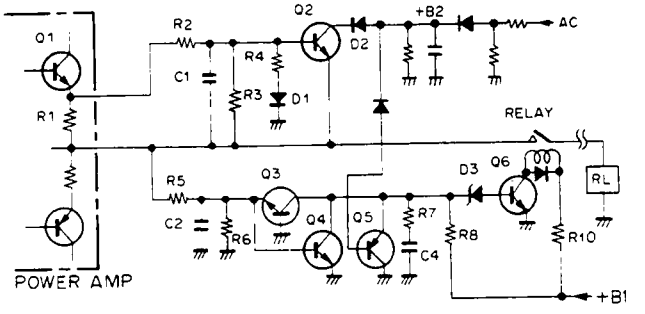


Fig. 4-24 Protection Circuit

4.9 PROTECTION CIRCUIT

The purpose of this circuit is to protect both the speakers and the power amplifiers. The relay in the output circuit is automatically opened in any of the following cases:

1. During the "transient operations" when the power supply is turned on and off.
2. Upon detection of a DC voltage in the output circuit, caused by component failure or accident.
3. Upon detection of an overload, caused by a short circuit in the load.

Muting Operation when Power Supply is Turned On and Off

With reference to Fig. 4-24 when the power supply is turned on, Q5 turns off due to +B2 (The time constant of the +B2 circuit is very small.). If there is no input (DC) on Q3 and Q4, they will be off, and the timing capacitor C4 charges up through R8 and R7, and thus Q6 turns on. When Q6 conducts, the relay operates, and the output muting on the power amplifier will be removed.

When the power supply is turned off, +B will abruptly decay, and Q5 will conduct. As a result, C4 will rapidly discharge, Q6 will cease to conduct, whereupon the relay will become de-energized and restore muting.

DC Voltage Detector

The output circuit is connected to the Q3 emitter and Q4 base via a low-pass filter (R5, C2). Any DC voltages appearing the output circuit of the power amplifier, it will be applied to the Q3 emitter and Q4 base. If the voltage is positive, Q4

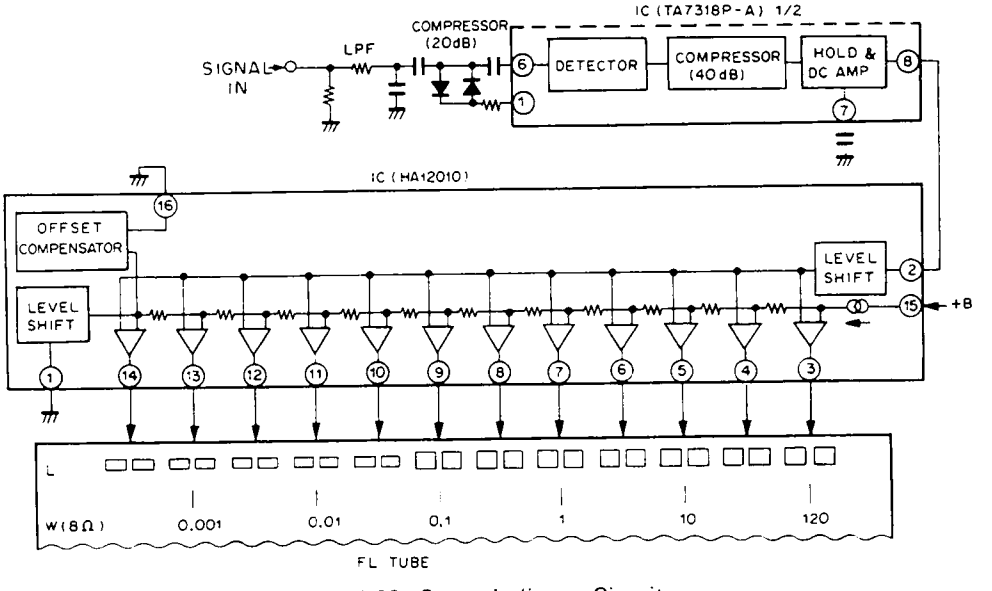


Fig. 4-23 Power Indicator Circuit

turns on. C4 will rapidly discharge. If the voltage is negative, Q3 turns on. C4 will rapidly discharge. As consequence, Q6 will turn off and the relay will become de-energized, thus causing the output circuit to open.

Overload Detection

The overload detector circuit incorporates the load (RL) in one side of a Wheatstone bridge (see Fig. 4-25). The base and emitter of a sensing transistor (Q2) are connected to the opposite corners of the bridge, so if RL decreases, Q2 will become forward biased. If RL falls below a prescribed value, Q2 will conduct, and Q5 will turn on. C4 will rapidly discharge. As consequence, Q6 will turn off and the relay will become re-energized, thus causing the output circuit to open.

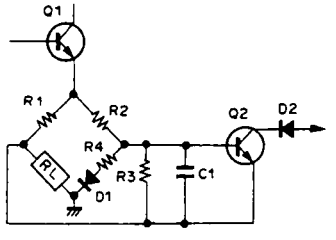


Fig. 4-25 Overload Detector

4.10 SURGE CURRENT SUPPRESSOR

Since the SX-D7000 employs a large toroidal power transformer and two 15,000μF capacitors in the power supply circuit, the sudden surge of current when the power supply is turned on may reach several hundred amperes. The surge current suppressor circuit used to reduce this sudden surge is shown in Fig. 4-26.

When the power switch (S1) is OFF (i.e. no supply of AC power), the relay contact (S2) is open. But when this switch (S1) is turned ON, the sudden surge of current is passed through R1, thereby greatly reducing the flow of current. When the output DC voltage of the power supply circuit reaches a certain prescribed level, S2 will close, and R1 consequently by-passed. The time required for this to occur, however, is considerably shorter than the time required for the muting circuit to operate when the power supply is turned on, so there is no undue effect upon normal operation of the receiver.

Microtemp is a temperature-sensitive fuse coupled to R1. If S2 fails to close due to an abnormality in the power supply circuit or relay, the heat generated in R1 will cause Microtemp to below, thereby opening the primary circuit.

When the POWER switch (S1) is turned OFF, the relay driving circuit is opened, thereby opening S2 and the primary circuit.

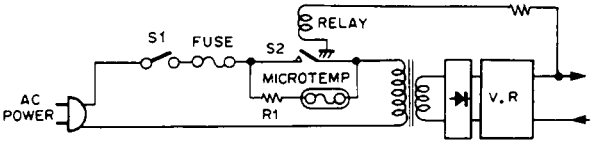


Fig. 4-26 Surge Current Suppressor Circuit

6. ADJUSTMENTS

6.1 TUNER SECTION

FM Tuner (Refer to Fig. 6-1)

- Connect the FM SG (FM signal generator) to the FM ANTENNA 300Ω terminal via 300Ω dummy antenna.
- Set the FM switch (FUNCTION) to the ON position, FM/AM MUTE switch to the OFF position.

Step	FM SG (400Hz, ±75kHz DEV.)		Frequency on the display	Adjustment point	Adjustment method
	Frequency	Level			
1	No signal		87.50MHz	L4	Obtain a reading of DC 6V between terminals no. 61 and no. 60 (ground).
2			108.00MHz	TC4	Obtain a reading of DC 20V between terminals no. 61 and no. 60 (ground).
3	Repeat steps 1 and 2 until both requirements are satisfied.				
4	90MHz	20dB	90.00MHz	L1	Obtain maximum DC voltage reading between terminal no. 6 and ground.
5				L2	
6				L3	
7	106MHz	20dB	106.00MHz	TC1	
8				TC2	
9				TC3	
10	Repeat steps 4 to 9 until the maximum sensitivity.				
11	98MHz	20dB	98.00MHz	T1	Obtain maximum DC voltage reading between terminal no.6 and ground.
12	No signal			T2-N	Obtain a reading of DC 0V between terminals no. 50 and no. 58.
13	98.000MHz*	66dB	98.00MHz	TC7	Obtain a reading of DC 0V between terminals no. 50 and no. 58.
14	98.000MHz*	66dB	98.00MHz	T2-D	Obtain minimum distortion in the demodulated output (TAPE REC terminal).
15	Repeat steps 12 to 14 until both requirements are satisfied.				
16	Set the FM/AM MUTE switch to the ON position.				
17	98MHz	36dB	98.00MHz	VR1	Obtain a position just prior to activation of the muting circuit.
18	98MHz	66dB	98.00MHz	VR5	Obtain a light up all points in the SIGNAL indicator (5-points display).

** This frequency needs exactitude.*

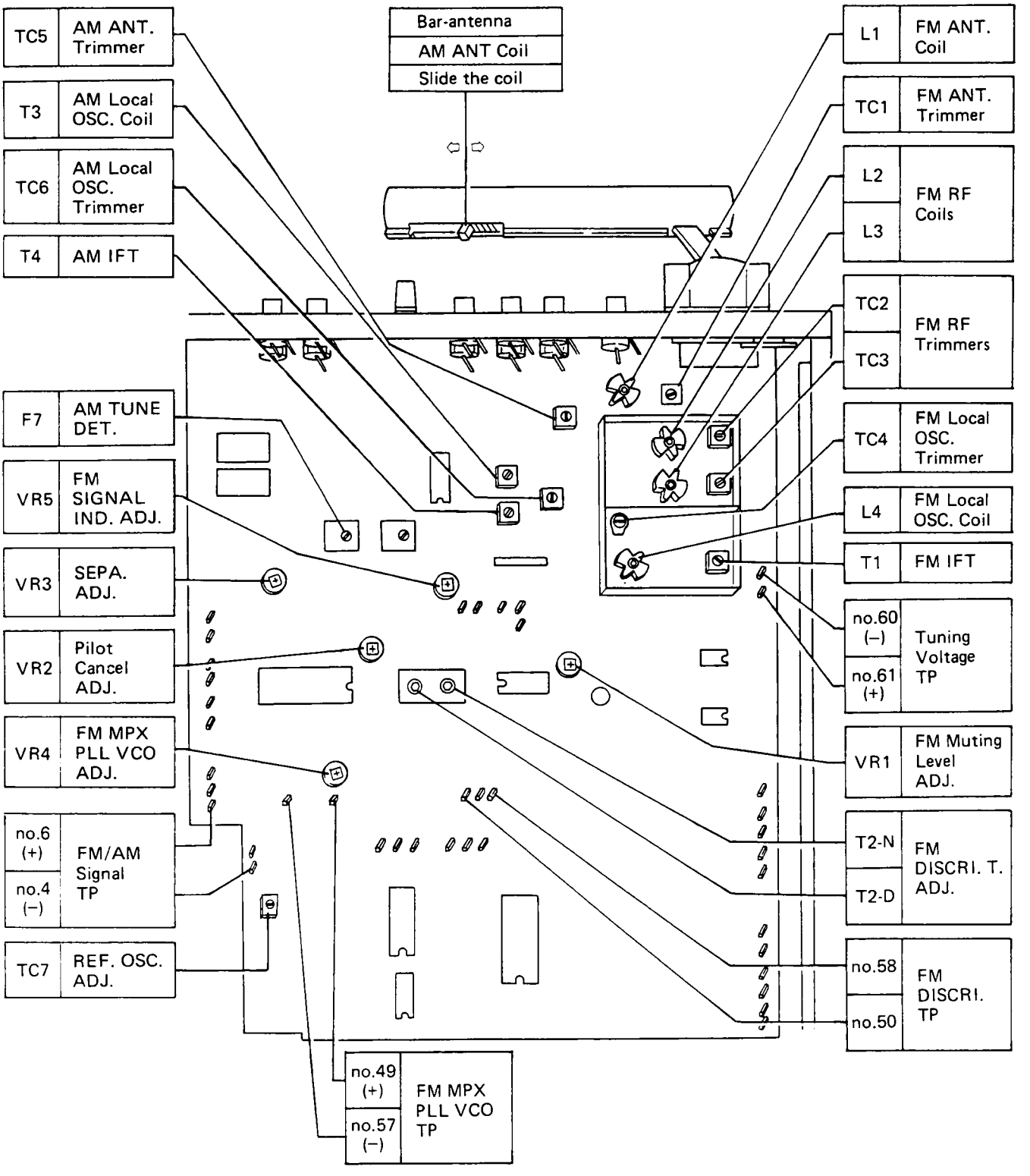


Fig. 6-1 Adjustment Points and Measuring Points

FM Multiplex Decoder Circuit

- Connect the MPX SG (FM multiplex signal generator) to the FM SG external modulator terminal.
- Set the FM SG output to 98.000MHz, and 86dB (modulation mode to external), and tune the SX-D7000 to this position (98.00MHz).

Step	FM MPX SG	Adjustment point	Adjustment method
1	No signal (unmodulated)	VR4	Obtain a 76kHz (within ±250Hz) signal at terminals no. 49 and no. 57 (ground).
2	Pilot (19kHz, ±7.5kHz DEV.) only	VR2	Obtain minimum leakage of the 19kHz pilot signal at the output (TAPE REC terminal).
3	Main (1kHz, L+R, ±67.5kHz DEV.) Pilot (19kHz, ±7.5kHz DEV.)	T1 (by up to 90° in either direction)	Reduce distortion in the output (TAPE REC terminal) to a minimum.
4	Main (1kHz, L or R, ±33.75kHz DEV.) Pilot (19kHz, ±7.5kHz DEV.)	VR3	Obtain minumum cross talk between left and right channels at the output (TAPE REC terminal).

AM Tuner

- Connect the AM SG (AM signal generator) to the AM ANTENNA terminal via 1kΩ resistor.
- Set the AM switch (FUNCTION) to the ON position, FM/AM MUTE switch to the OFF position.
- Set the AM CHANNEL STEP selector to the 10kHz position.

Step	AM SG (400Hz, 30% MOD.)		Frequency on the display	Adjustment point	Adjustment method
	Frequency	Level			
1	No signal		525kHz	T3	Obtain a reading of DC 2V between terminals no. 61 and no. 60 (ground).
2			1605kHz	TC6	Obtain a reading of DC 25V between terminals no. 61 and no. 60 (ground).
3	Repeat steps 1 and 2 until both requirements are satisfied.				
4	600kHz	40dB	600kHz	Bar-antenna	Obtain maximum DC voltage reading between terminal no. 6 and ground.
5	1400kHz	40dB	1400kHz	TC5	
6	Repeat steps 4 and 5 until the maximum sensitivity.				
7	1000kHz	40dB	1000kHz	T4	Obtain maximum DC voltage reading between terminal no.6 and ground.
8				F7	

6.2 AUDIO SECTION

Power Amplifier

- Turn VR3, VR5 (L) and VR4, VR6 (R) fully around in the counter-clockwise direction, but set VR1 (L) and VR2 (R) to the center positions.
- Without any load or input signal, turn the POWER switch ON.

Adjustment point	Prescribed value	Measuring terminals
DC Balance		
VR1(L)	DC 0V ±30mV	Output terminals (SPEAKERS)
VR2(R)	DC 0V ±30mV	
Idle Current		
VR3(L)	DC 56mV	JP13(+) and JP15
VR5(L)	DC 70mV	
VR4(R)	DC 56mV	JP25(+) and JP23
VR6(R)	DC 70mV	

Output Power Indicator Calibration

1. Apply a 1kHz signal to the POWER AMP IN terminals (or any other input power amplifier input terminals).
2. Adjust the level of this input signal so that the voltage on the output terminals (SPEAKERS) read 8.95V (rms).
3. Adjust VR2 (L) and VR1 (R) so that the output power indicators read 10 watts.

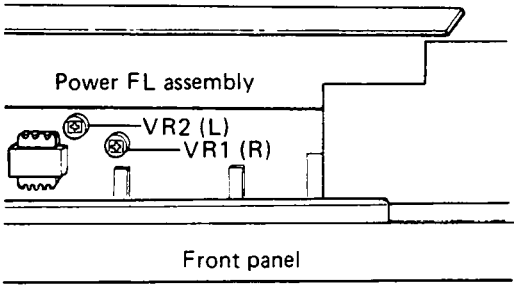


Fig. 6-3 Adjustment Points

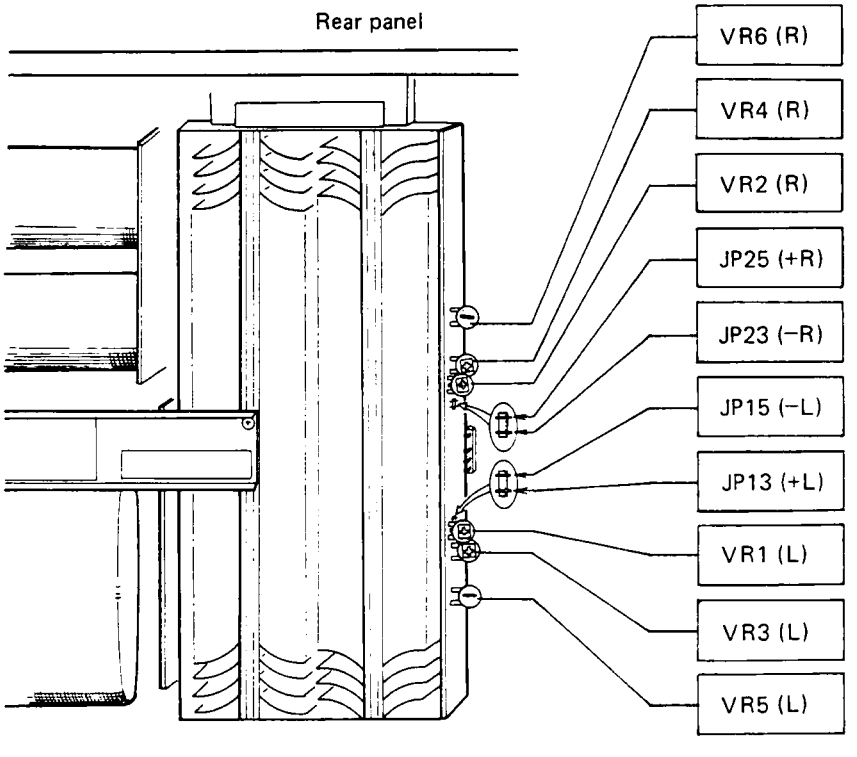
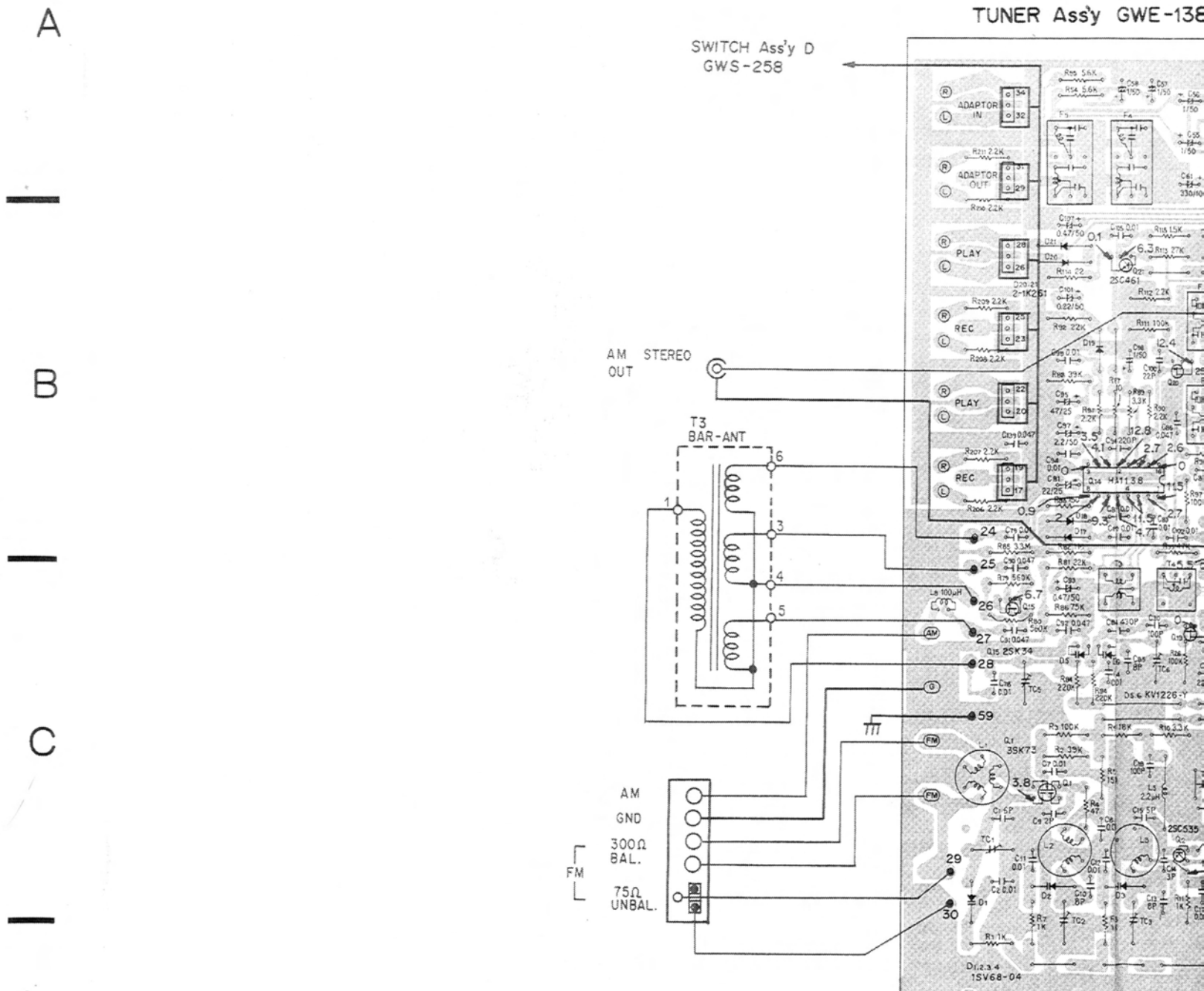
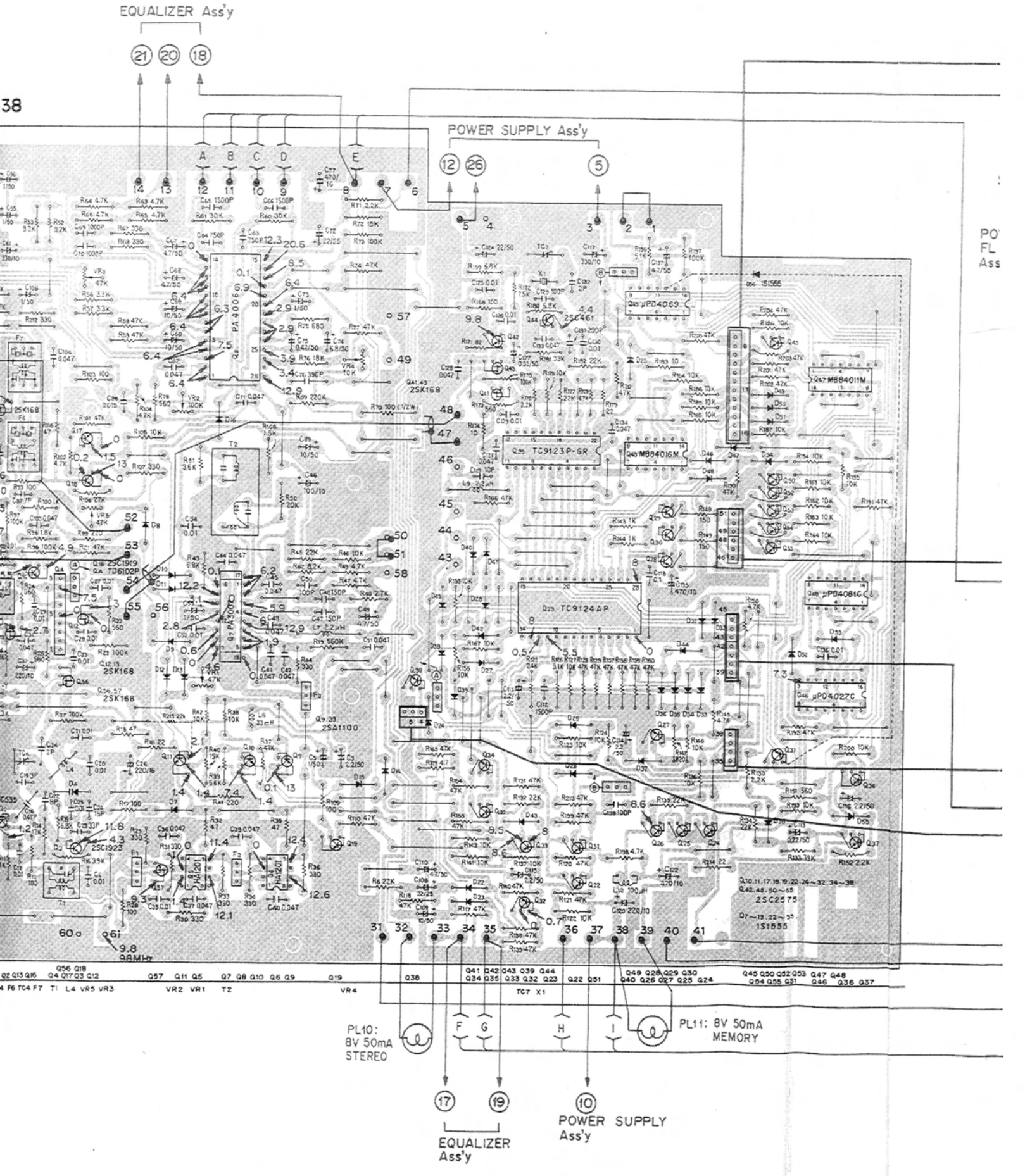


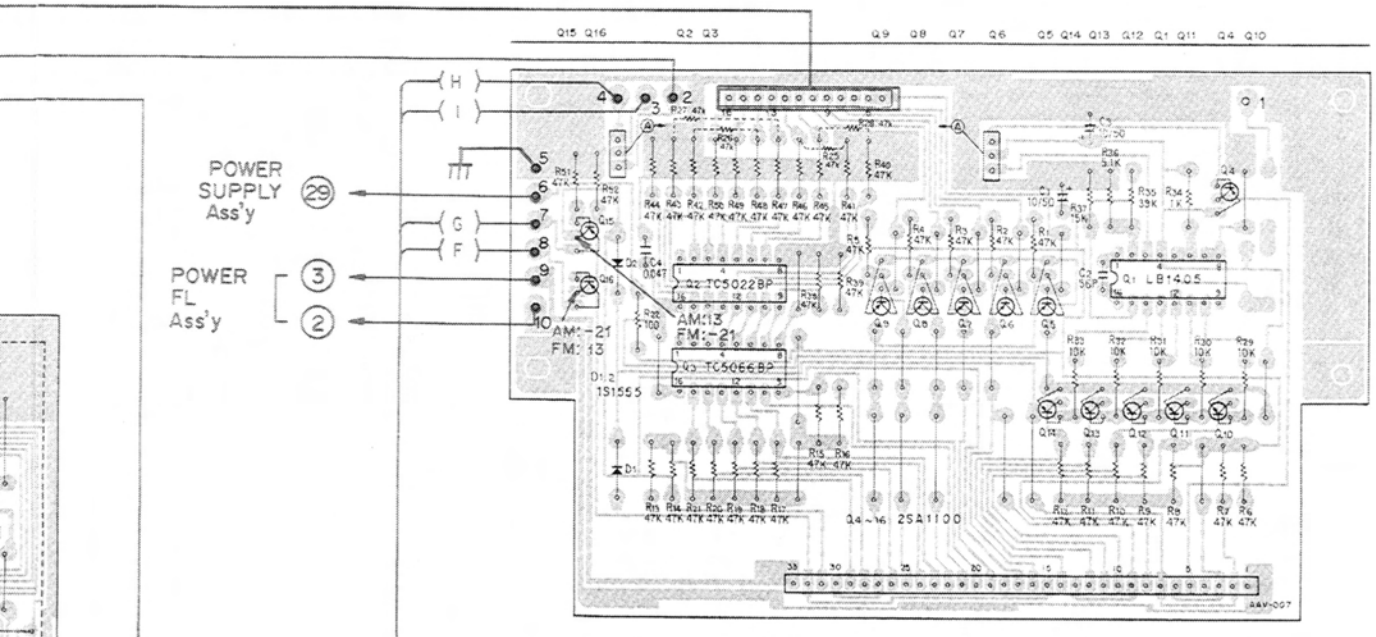
Fig. 6-2 Adjustment Points and Measuring Points

8. P.C. BOARD PATTERNS AND SCHEMATIC DIAGRAMS

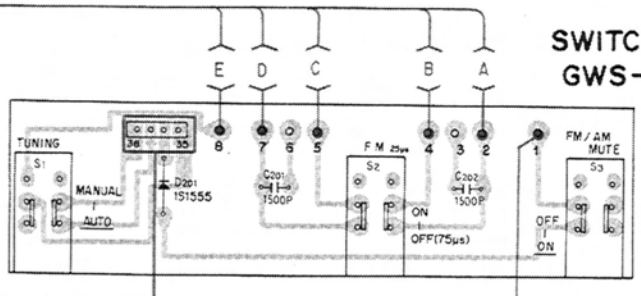
8.1 P.C. BOARDS CONNECTION DIAGRAM (TUNER SECTION)



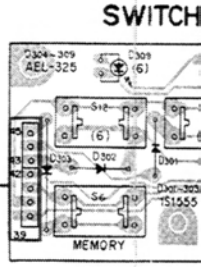

EQUALIZER Ass'y
21 20 18
POWER SUPPLY Ass'y
12 26 5
A B C D E
14 13 12 11 10 9 8 7 6
5 4 3 2 1
PA4006
Q25 TC9123P-GR
Q40 M884016M
Q25 TC9124AP
Q46 μPD4027C
Q49 μPD4081C
Q47 M884011M
2SK168
2SA1100
2SC1923
2SC2575
TD6102P
1S1555
PL10: 8V 50mA STEREO
PL11: 8V 50mA MEMORY
31 32 33 34 35 36 37 38 39 40 41
F G H I
17 19
EQUALIZER Ass'y
10
POWER SUPPLY Ass'y



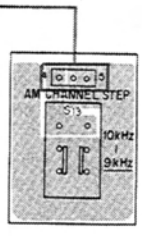
COUNTER FL Ass'y AWV-015



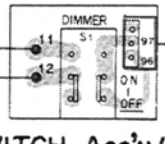
SWITCH Ass'y (B)
GWS-260



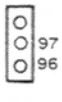
SWITCH



SWITCH Ass'y (C)
GWS-261



POWER FL Ass'y



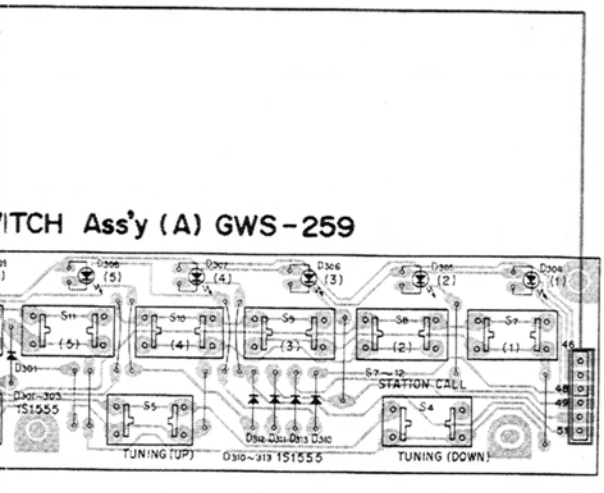
SWITCH Ass'y (E)
GWS-262

A

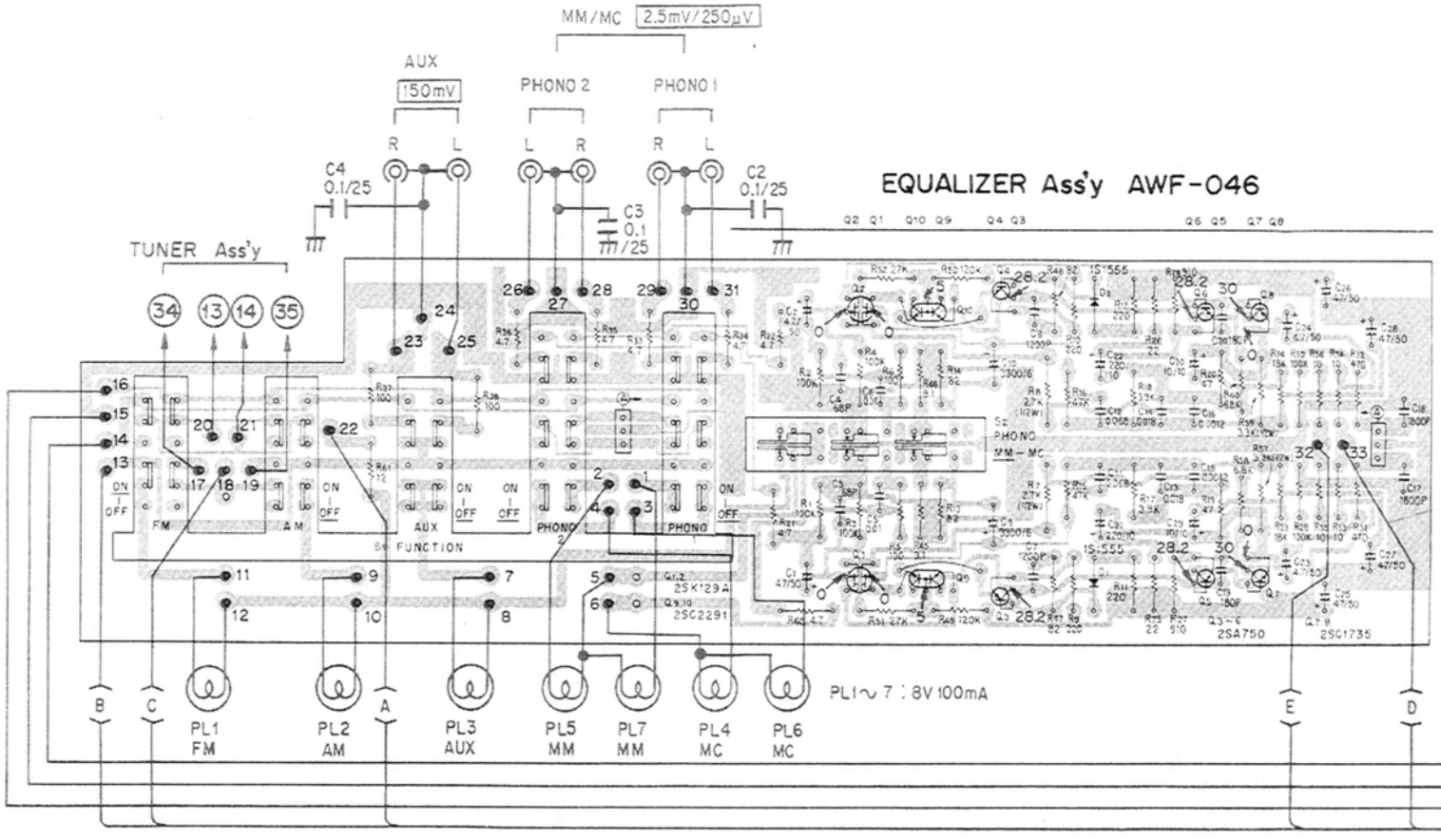
B

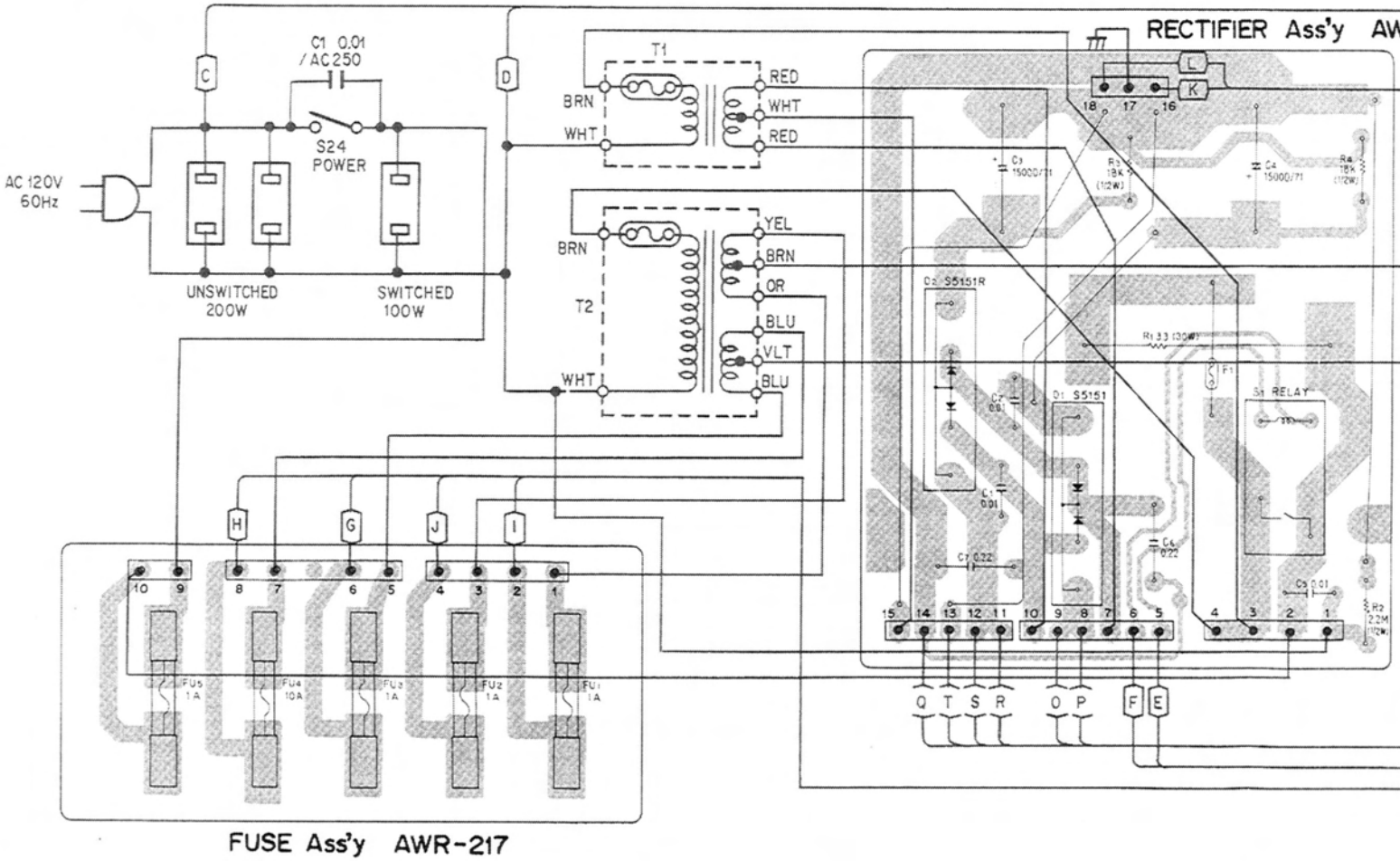
C

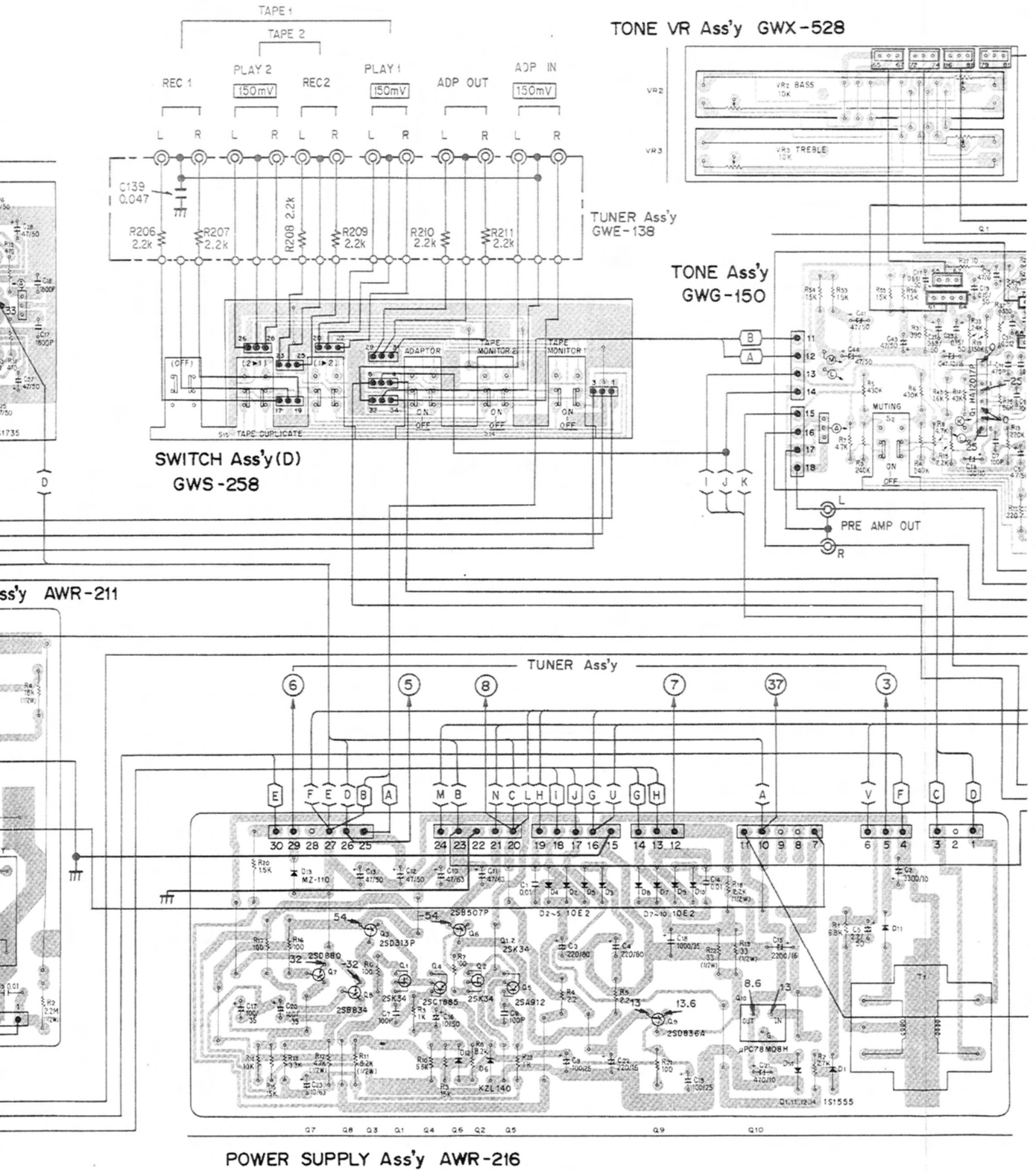
D


ITCH Ass'y (A) GWS-259
D306 (5)
D307 (4)
D308 (3)
D309 (2)
D304 (1)
S11
S10
S9
S8
S7
S6
S5
S4
S7~12
STATION CALL
TUNING (UP)
TUNING (DOWN)
D310~313 1S1555

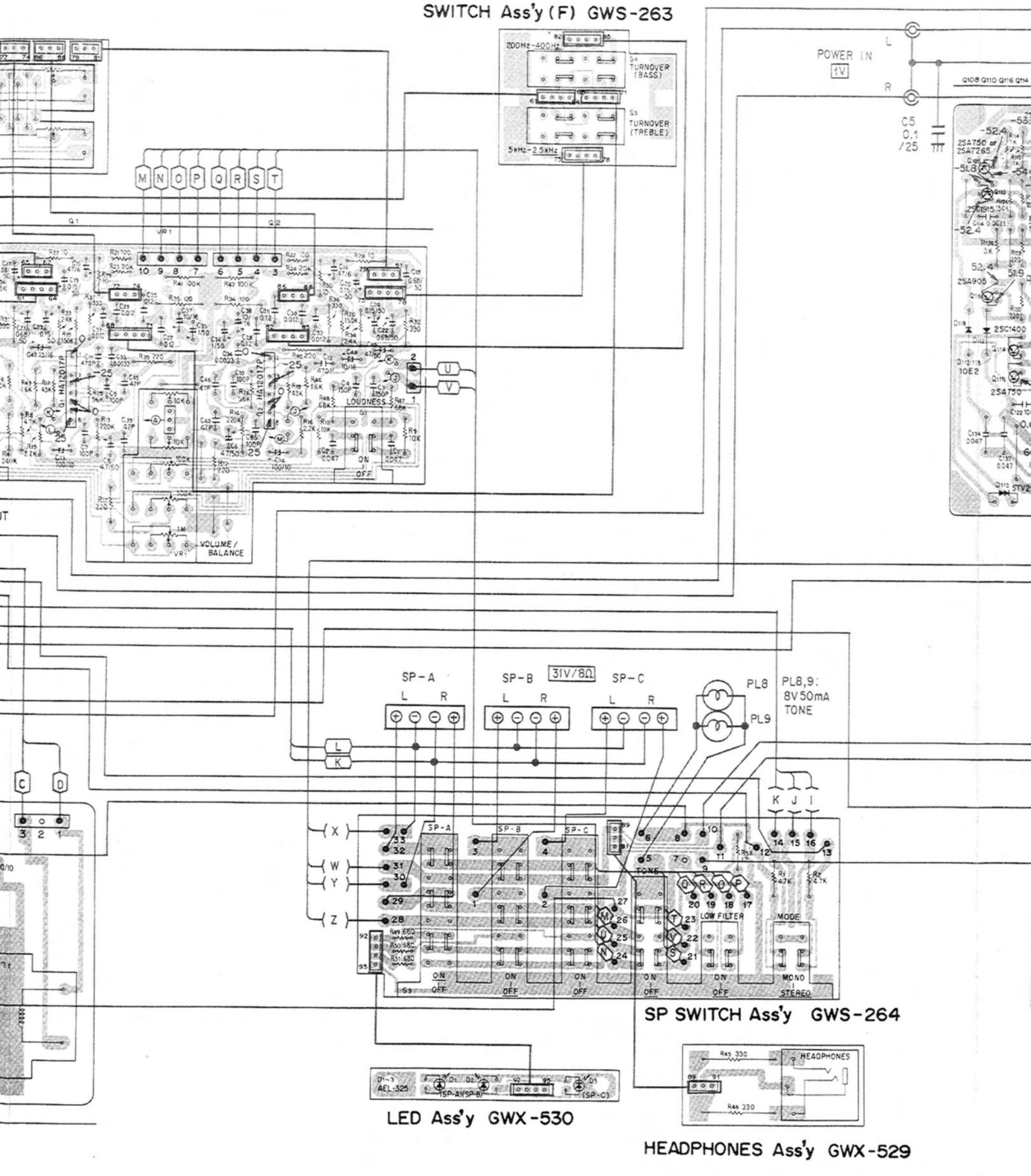
8.3 P.C. BOARDS CONNECTION DIAGRAM (AUDIO SECTION)

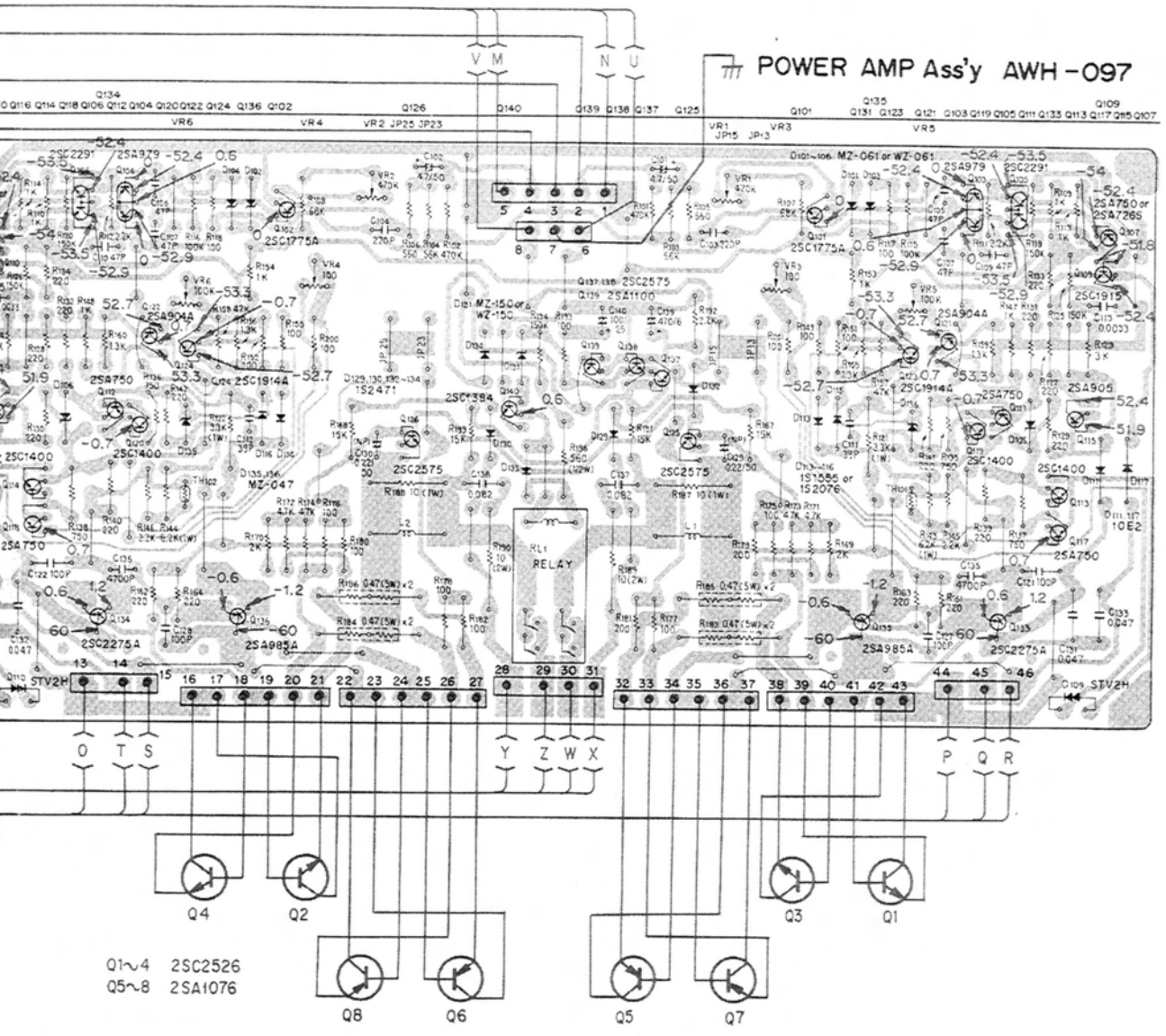


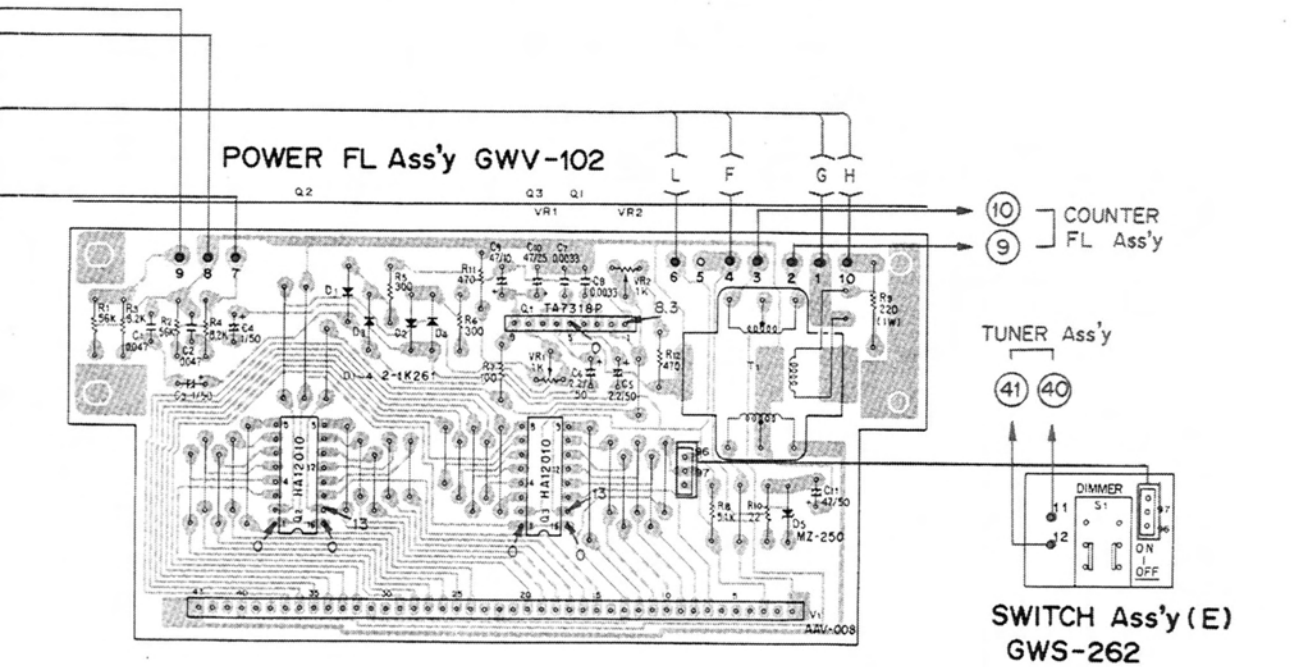



TAPE 1
TAPE 2
REC 1
PLAY 2
150mV
REC2
PLAY 1
150mV
ADP OUT
ADP IN
150mV
L R L R L R L R L R L R
C139 0.047
R206 2.2k
R207 2.2k
R208 2.2k
R209 2.2k
R210 2.2k
R211 2.2k
TUNER Ass'y GWE-138
TONE VR Ass'y GWX-528
VR2 BASS 10K
VR3 TREBLE 10K
TONE Ass'y GWG-150
MUTING
PRE AMP OUT
SWITCH Ass'y(D) GWS-258
TAPE DUPLICATE
ADAPTOR
TAPE MONITOR 2
TAPE MONITOR 1
ON OFF
Ass'y AWR-211
TUNER Ass'y
POWER SUPPLY Ass'y AWR-216
2SB507P
2SD313P
2SD880
2SB834
2SK34
2SC1885
2SA912
2SD836A
KZL140
μPC78M08H
1S1555

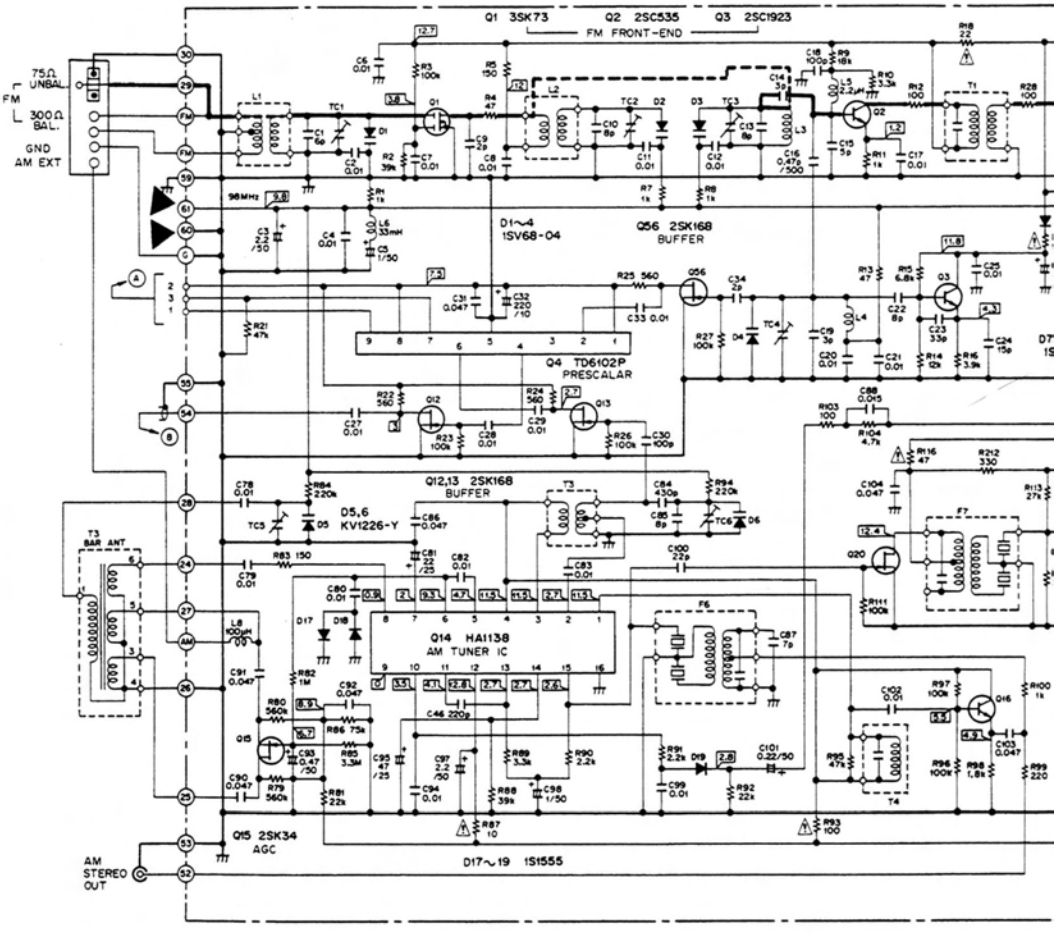
SWITCH Ass'y (F) GWS-263

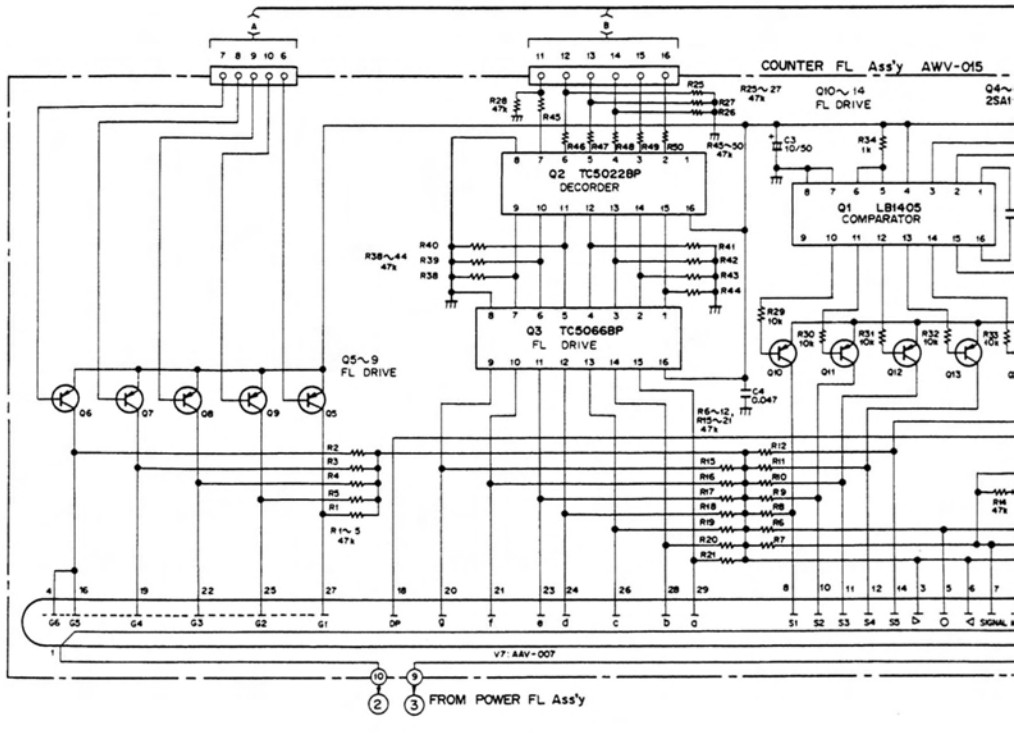


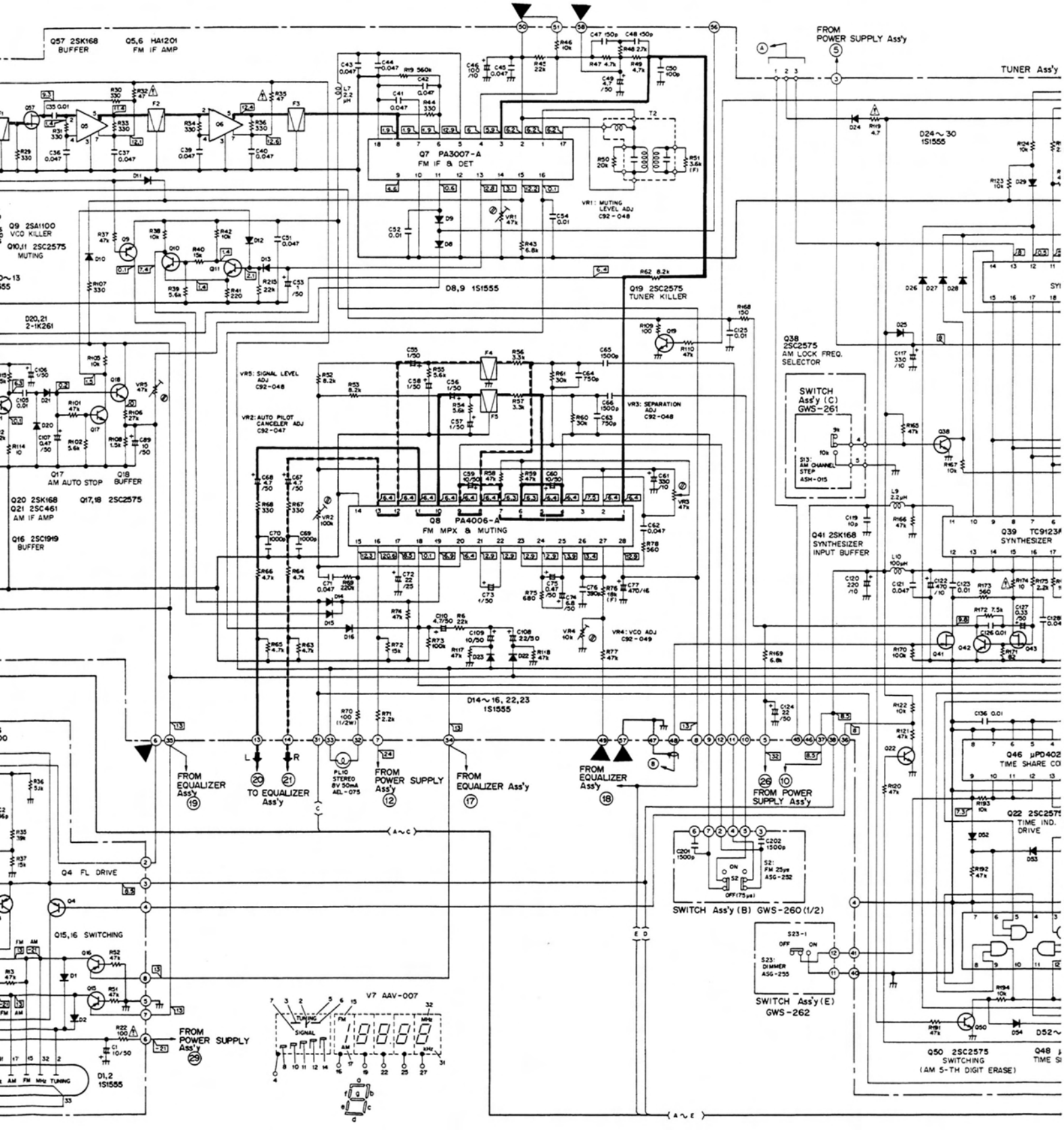

POWER AMP Ass'y AWH-097
RELAY
STV2H
STV2H
Q1~4 2SC2526
Q5~8 2SA1076
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8


POWER FL Ass'y GWV-102
COUNTER FL Ass'y
TUNER Ass'y
DIMMER
ON
OFF
SWITCH Ass'y (E)
GWS-262

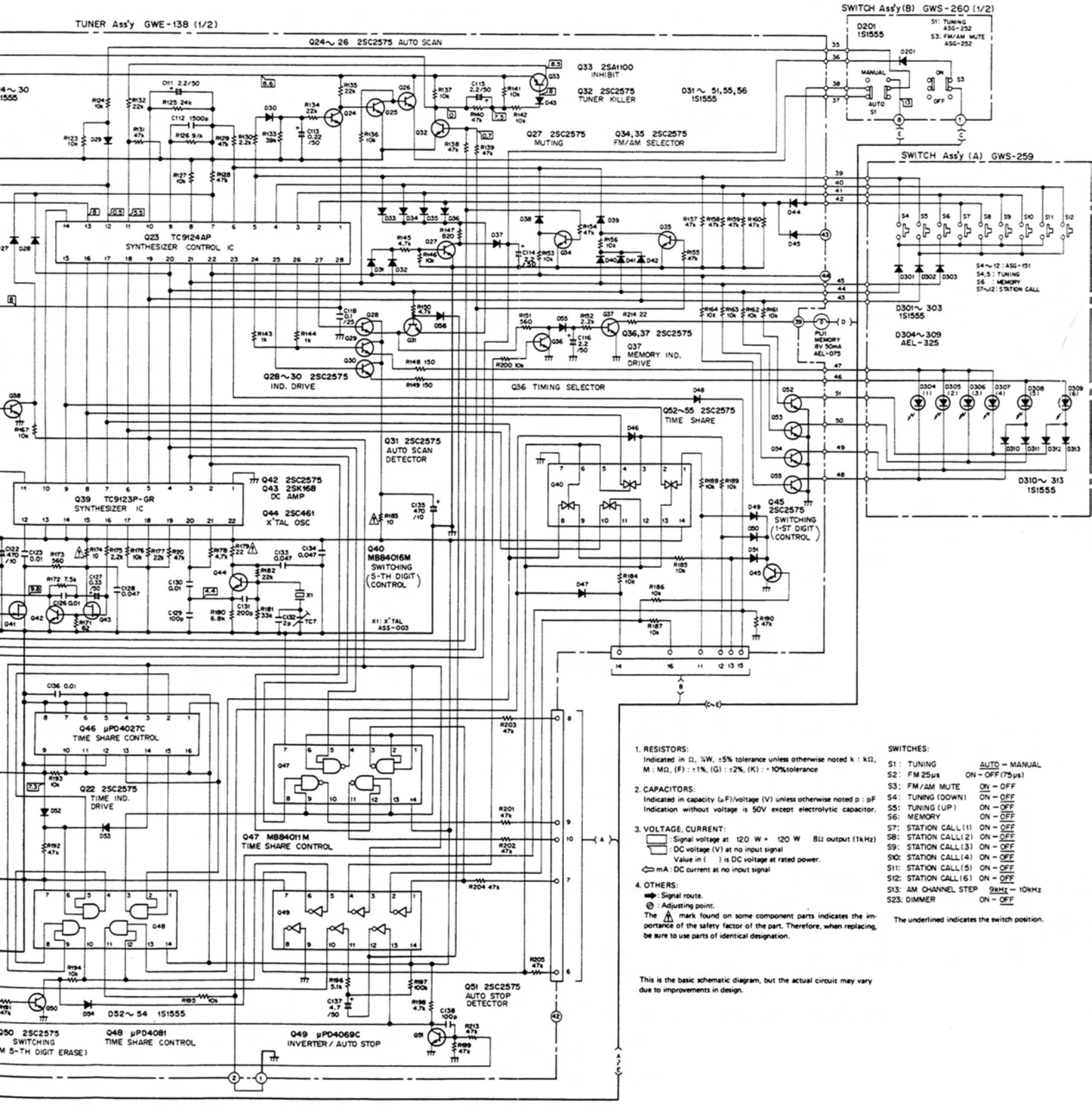
8.2 SCHEMATIC DIAGRAM (TUNER SECTION)






Q57 2SK168 BUFFER
Q5,6 HA1201 FM IF AMP
Q7 PA3007-A FM IF & DET
FROM POWER SUPPLY Ass'y
TUNER Ass'y
D24~30 1S1555
D8,9 1S1555
Q19 2SC2575 TUNER KILLER
Q9 2SA1100 VCO KILLER
Q10,11 2SC2575 MUTING
D20,21 2-1K261
VR1: MUTING LEVEL ADJ C92-048
VR2: AUTO PILOT CANCELER ADJ C92-047
VR3: SEPARATION ADJ C92-048
VR5: SIGNAL LEVEL ADJ C92-048
Q38 2SC2575 AM LOCK FREQ. SELECTOR
SWITCH Ass'y (C) GWS-261
Q8 PA4006-A FM MPX & MUTING
Q17 AM AUTO STOP
Q18 BUFFER
Q20 2SK168 Q21 2SC461 AM IF AMP
Q17,18 2SC2575
Q16 2SC1919 BUFFER
Q41 2SK168 SYNTHESIZER INPUT BUFFER
Q39 TC9123 SYNTHESIZER
VR4: VCO ADJ C92-049
D14~16, 22, 23 1S1555
FROM EQUALIZER Ass'y
TO EQUALIZER Ass'y
FROM POWER SUPPLY Ass'y
FROM EQUALIZER Ass'y
FROM EQUALIZER Ass'y
FROM POWER SUPPLY Ass'y
Q4 FL DRIVE
Q15,16 SWITCHING
SWITCH Ass'y (B) GWS-260 (1/2)
SWITCH Ass'y (E) GWS-262
V7 AAV-007
D1,2 1S1555
Q50 2SC2575 SWITCHING (AM 5-TH DIGIT ERASE)
Q46 μPD402 TIME SHARE CO
Q22 2SC257 TIME IND. DRIVE

NOTE:
The indicated semiconductors are represe
only. Other alternative semiconductors may
are listed in the parts list.



1. RESISTORS:
Indicated in Ω, ¼W, ±5% tolerance unless otherwise noted k : kΩ, M : MΩ, (F) : ±1%, (G) : ±2%, (K) : ±10%tolerance

2. CAPACITORS:
Indicated in capacity (μF)/voltage (V) unless otherwise noted p : pF
Indication without voltage is 50V except electrolytic capacitor.

3. VOLTAGE, CURRENT:
: Signal voltage at 120 W + 120 W 8Ω output (1kHz)
: DC voltage (V) at no input signal
Value in ( ) is DC voltage at rated power.
⇦mA : DC current at no input signal

4. OTHERS:
➡: Signal route.
⊘ : Adjusting point.
The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.

This is the basic schematic diagram, but the actual circuit may vary due to improvements in design.

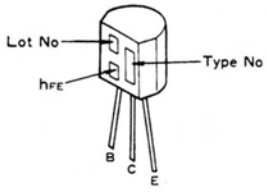
SWITCHES:

S1:	TUNING	AUTO – MANUAL
S2:	FM 25μs	ON – OFF (75μs)
S3:	FM/AM MUTE	ON – OFF
S4:	TUNING (DOWN)	ON – OFF
S5:	TUNING (UP)	ON – OFF
S6:	MEMORY	ON – OFF
S7:	STATION CALL (1)	ON – OFF
S8:	STATION CALL (2)	ON – OFF
S9:	STATION CALL (3)	ON – OFF
S10:	STATION CALL (4)	ON – OFF
S11:	STATION CALL (5)	ON – OFF
S12:	STATION CALL (6)	ON – OFF
S13:	AM CHANNEL STEP	9kHz – 10kHz
S23:	DIMMER	ON – OFF

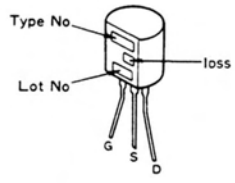
The underlined indicates the switch position.

presentative ones may be used and

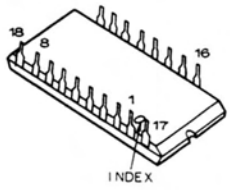
2SA1100
2SC1919
2SC2575



2SK168

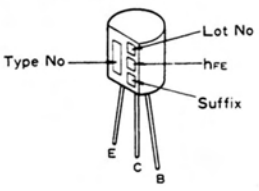


PA3007-A

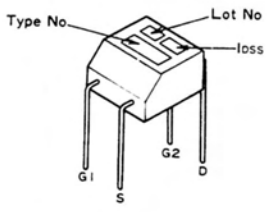


A

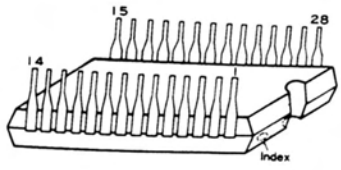
2SA733A
2SC945A



3SK73

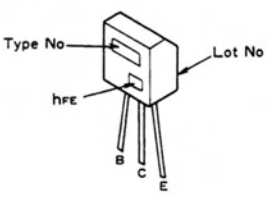


PA4006-A

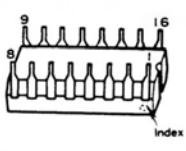


B

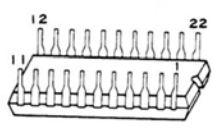
2SC461
2SC535



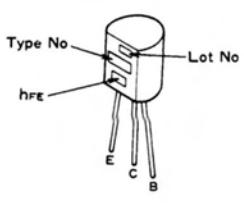
LB1405
TC5022BP
TC5066BP
HA1138
μPD4027C



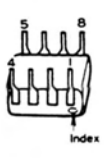
TC9123P-GR



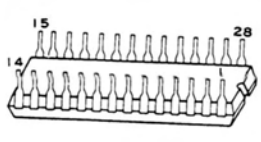
2SC1923



HA1201

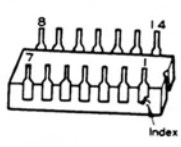


TC9124AP

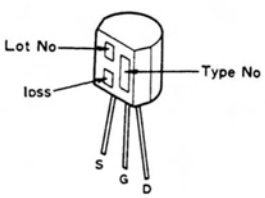


C

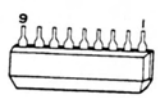
MB84011M
MB84016M
μPD4011C
μPD4081C
μPD4069C



2SK34



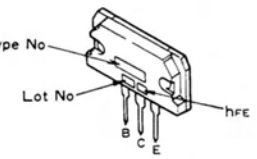
TD6102P



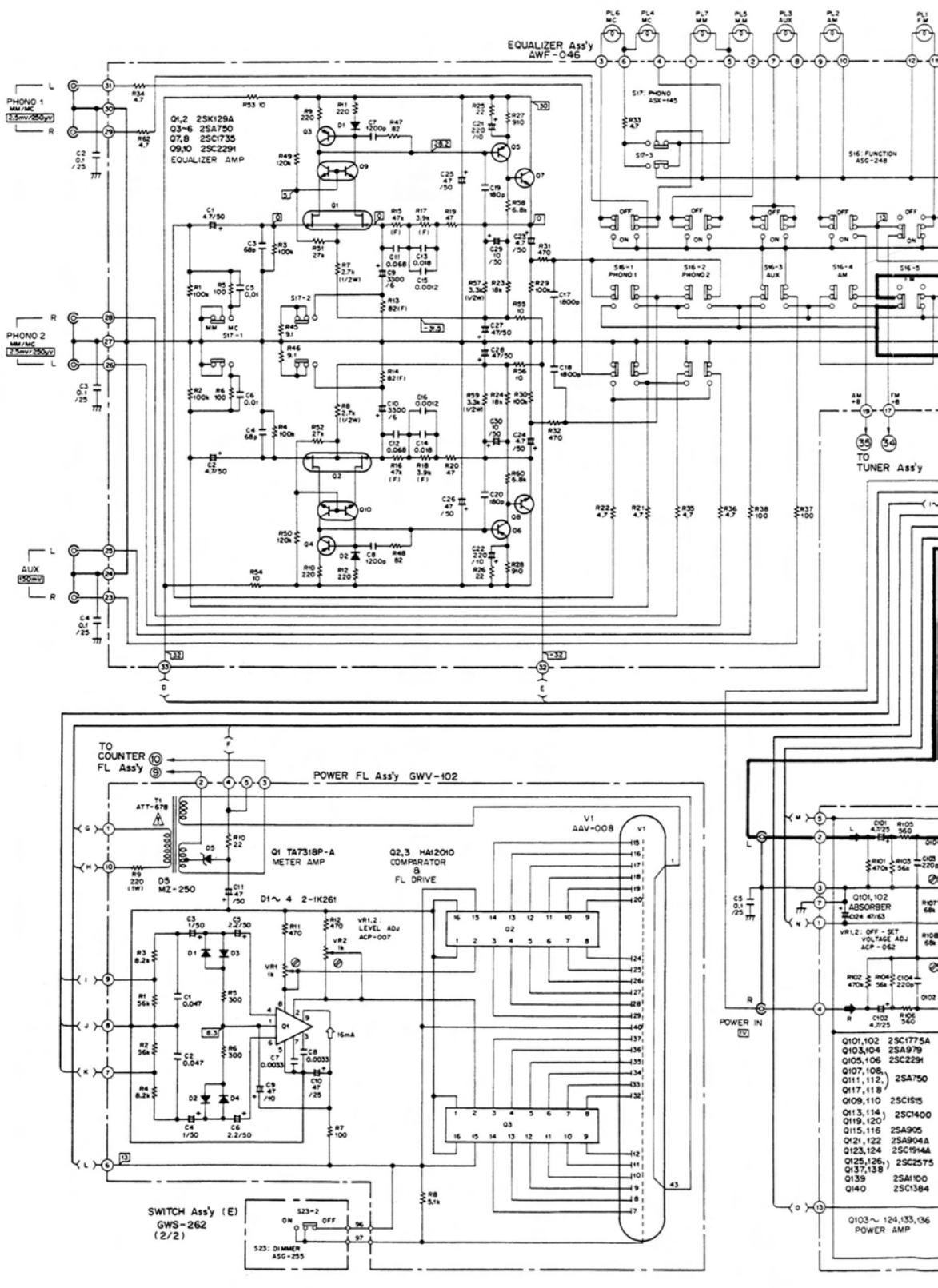
D

8.4 SCHEMATIC DIAGRAM (AUDIO SECTION)

2SA1076
2SC2526



2SA75
2SC14



4 5 6

2SA750
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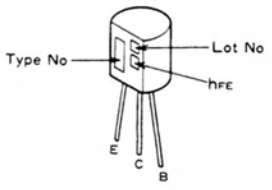
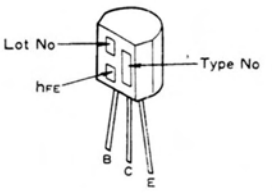
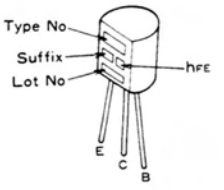
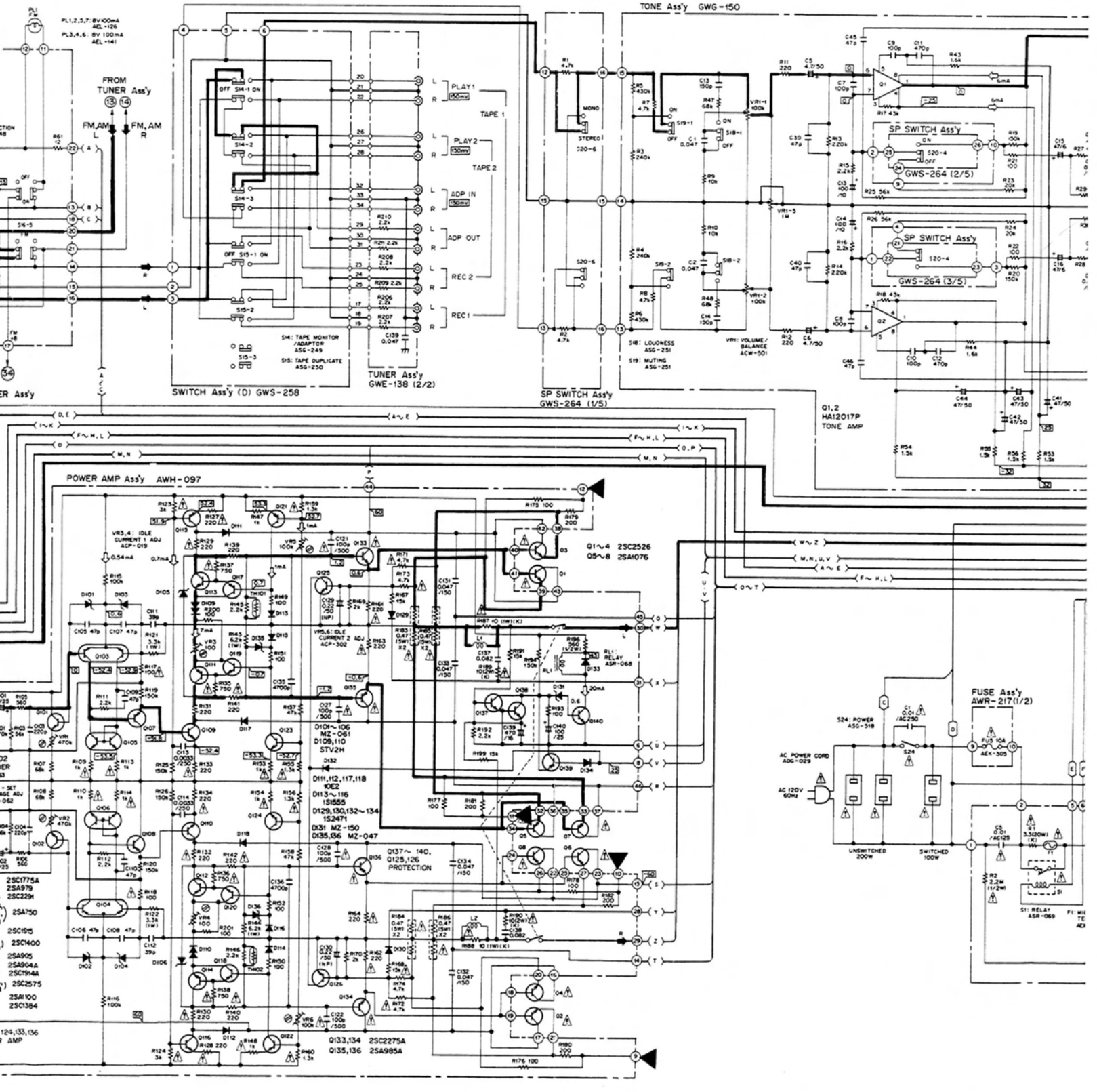


2SA726S
2SA1100
2SC2575



2SC1775A

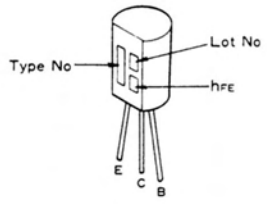




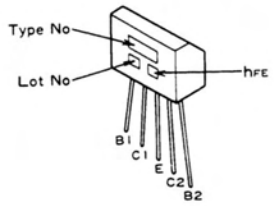
4 5 6

7 8 9

2SA912
2SC1885



2SA979



2SA905
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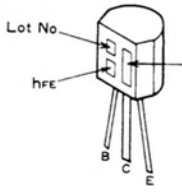
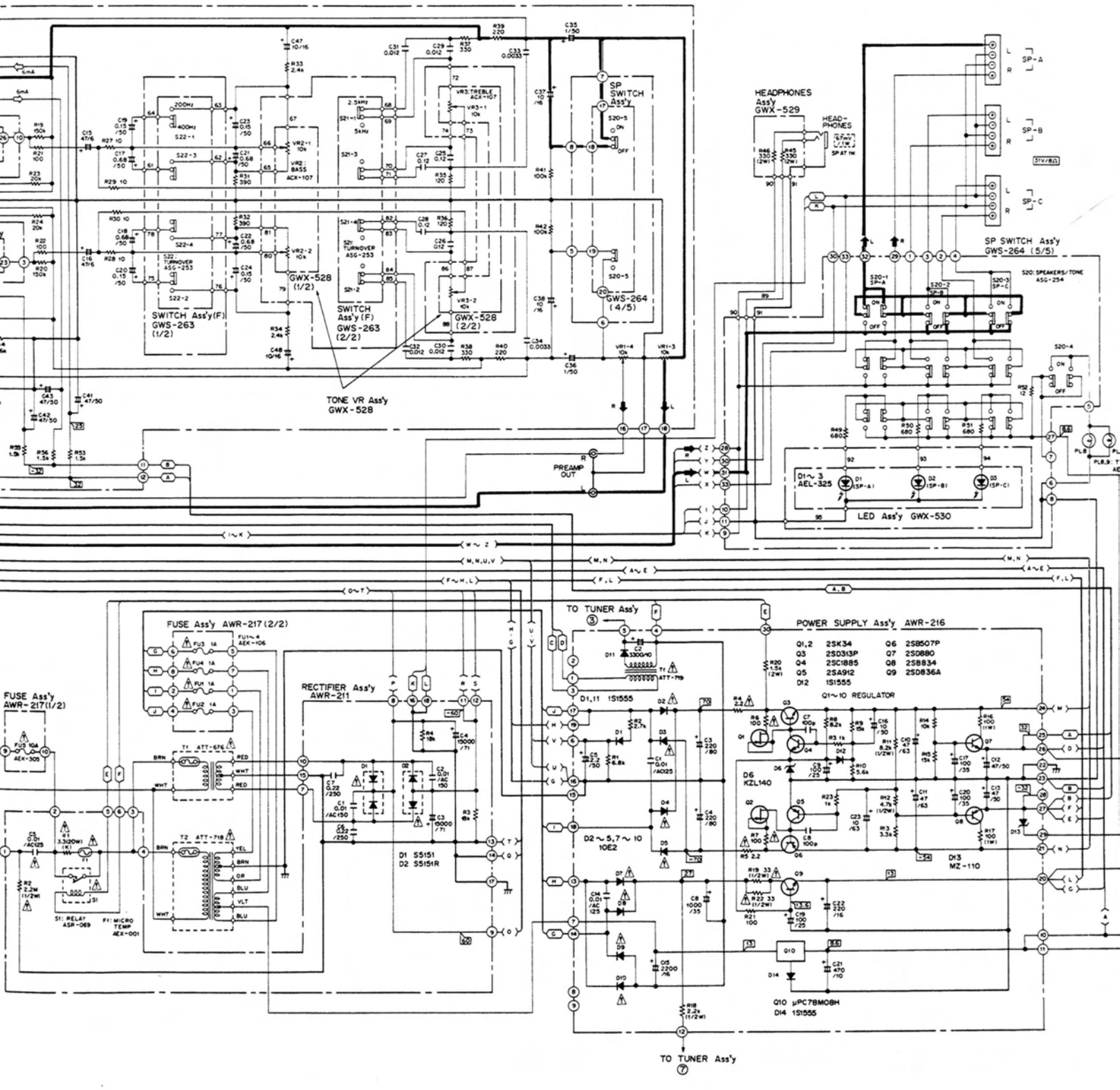
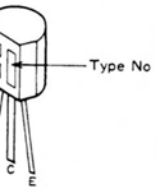
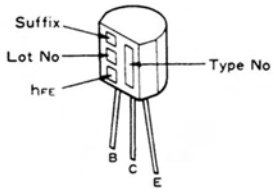




7 8 9



2SA904A
2SC1914A



1. RESISTORS:
Indicated in Ω, ¼W, ±5% tolerance unless otherwise noted k : kΩ, M : MΩ, (F) : ±1%, (G) : ±2%, (K) : ±10%tolerance

2. CAPACITORS:
Indicated in capacity (μF)/voltage (V) unless otherwise noted p : pF
Indication without voltage is 50V except electrolytic capacitor.

3. VOLTAGE, CURRENT:
Signal voltage at 120 W + 120 W 8Ω output (1kHz)
: DC voltage (V) at no input signal
Value in ( ) is DC voltage at rated power.
⇦mA: DC current at no input signal

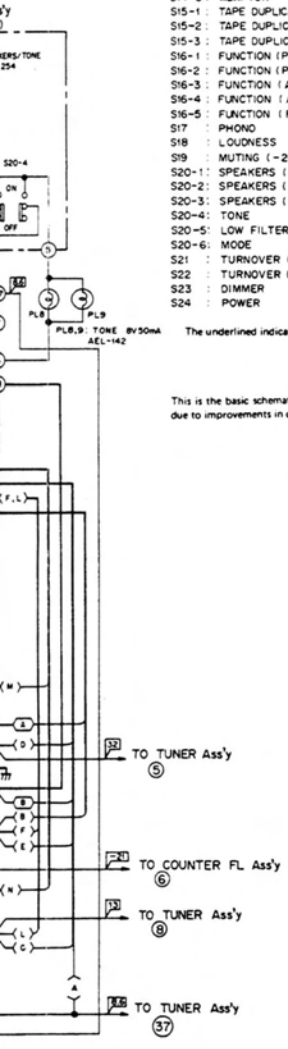
4. OTHERS:
➡ : Signal route.
⊘ : Adjusting point.
The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.

SWITCHES:

S14-1	TAPE MONITOR (1)	ON – OFF
S14-2	TAPE MONITOR (2)	ON – OFF
S14-3	ADAPTOR	ON – OFF
S15-1	TAPE DUPLICATE (1➡2)	ON – OFF
S15-2	TAPE DUPLICATE (2➡1)	ON – OFF
S15-3	TAPE DUPLICATE (OFF)	ON – OFF
S16-1	FUNCTION (PHONO 1)	ON – OFF
S16-2	FUNCTION (PHONO 2)	ON – OFF
S16-3	FUNCTION (AUX)	ON – OFF
S16-4	FUNCTION (AM)	ON – OFF
S16-5	FUNCTION (FM)	ON – OFF
S17	PHONO	MM – MC
S18	LOUDNESS	ON – OFF
S19	MUTING (–20dB)	ON – OFF
S20-1	SPEAKERS (A)	ON – OFF
S20-2	SPEAKERS (B)	ON – OFF
S20-3	SPEAKERS (C)	ON – OFF
S20-4	TONE	ON – OFF
S20-5	LOW FILTER	ON – OFF
S20-6	MODE	STEREO – MONO
S21	TURNOVER (TREBLE)	2.5kHz – 5kHz
S22	TURNOVER (BASS)	200Hz – 400Hz
S23	DIMMER	ON – OFF
S24	POWER	ON – STAND-BY

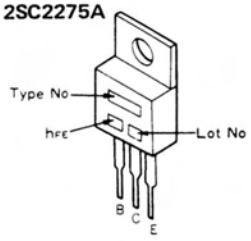
The underlined indicates the switch position.

This is the basic schematic diagram, but the actual circuit may vary due to improvements in design.

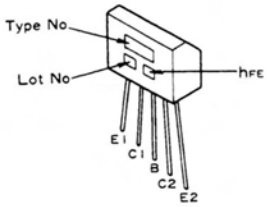


NOTE:
The indicated semiconductors are representative ones only. Other alternative semiconductors may be used and are listed in the parts list.

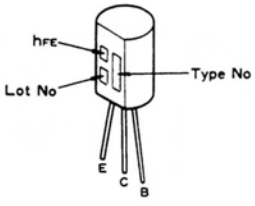
2SA985A
2SC2275A



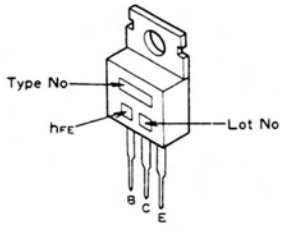
2SC2291



2SC1384



2SB834
2SD836A
2SD880



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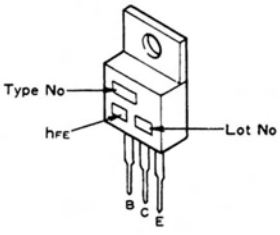

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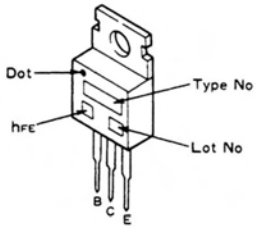

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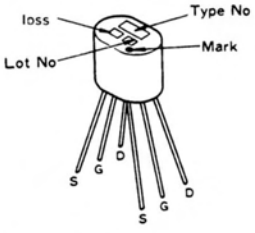

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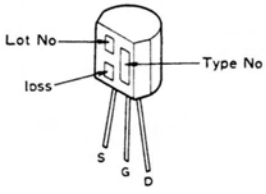
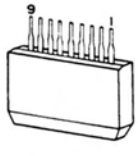


TA7318P-A



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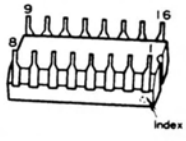

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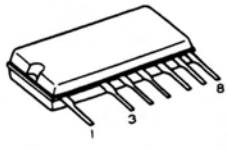

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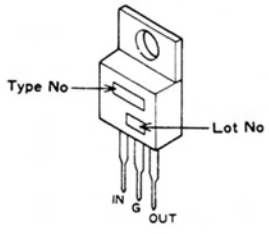

A B C D